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450726-000

MSI CONFIDENTIAL

UNDERDOG(MS-7500)

BTX(264.16mm X 266.4mm)

CPU:

AMD AM2R2+ Socket940

System Chipset:

North Bridge --- AMD-ATI RS780C

South Bridge --- AMD-ATI SB700

OnBoard Chipset:

Clock Gen:Seligo P625

AZALIA Codec:ADI1884

LAN(PHY):BOARDCOM 5754

SIO:SMSC 5327 (5764)

Flash ROM: 8 MB SPI (CHIP)

Main Memory:

DDRII (667/800MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 1

PCI Express (X1) Slot * 2

PCI Slot * 1

PWM:

Controller:ISL6323 (4-Phase 89W)

ACPI:

INTERSIL 6545

Other:

FDD *1

SATA(SATA2-300MB/s) *4

USB2.0 *10 (Rear*6 Front*4)

DVI*1

VGA PORT *1

PRINT Header *1

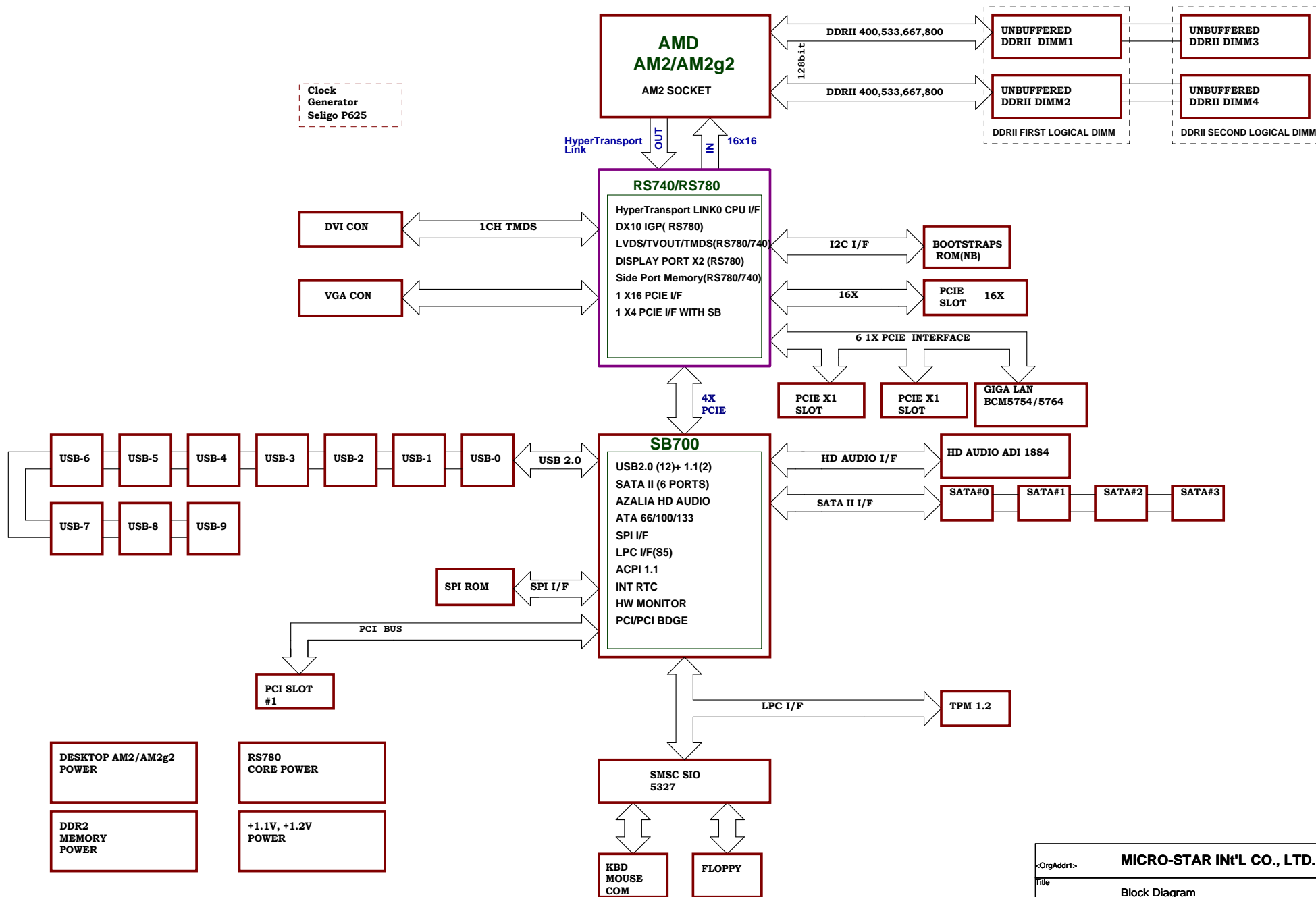
TPM *1

COM PORT *1

COM Header *1

MICRO-STAR INT'L CO., LTD.			
<OrgAddr1>		Title	
		Cover Sheet	
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RX780/RS780 + SB700 CUSTOMER DESKTOP REFERENCE DESIGN



DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 2 CH-A	10100000B	MEM_MAO_CLK_H0/L0 MEM_MAO_CLK_H1/L1 MEM_MAO_CLK_H2/L2
DIMM 4 CH-A	10100010B	MEM_MA1_CLK_H0/L0 MEM_MA1_CLK_H1/L1 MEM_MA1_CLK_H2/L2
DIMM 1 CH-B	10100001B	MEM_MBO_CLK_H0/L0 MEM_MBO_CLK_H1/L1 MEM_MBO_CLK_H2/L2
DIMM 3 CH-B	10100011B	MEM_MB1_CLK_H0/L0 MEM_MB1_CLK_H1/L1 MEM_MB1_CLK_H2/L2

USB	Port	DATA +/-	OC#
Rear	QUAD STACK	USB0- USB0+ USB1- USB1+ USB2- USB2+ USB3- USB3+	USB_OC#0 (OC#0~1)
	LAN_USB1	USB4- USB4+ USB5- USB5+	USB_OC#1 (OC#2)
Front	FRONT USB	USB6- USB6+ USB7- USB7+	USB_OC#2 (OC#3)
	MEDIA CARD READER	USB8- USB8+ USB9- USB9+	USB_OC#3 (OC#4)

PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INT#E PCI_INT#F PCI_INT#G PCI_INT#H	PCI_REQ0# PCI_GNT0#	AD20	PCICLK2_SLOT1 (PCICLK2)
TPM				LPCCLK0
SIO				LPCCLK1

PCI RESET DEVICE

SB 700	
Signals	Target
PCIRST#	PCISLOT1
PE_RST#	TPM_RST#
PE_RST#	LPC/SIO

TABLE 37
SIO8 GPIO ASSIGNMENTS

SIO GPIO	Function	Comment
GP 11	CHAFAN_PWM	Chassis Fan PWM command input, install 1K PU to +3.3 V
GP 12	RC_ID	Multi-state GPIO
GP 13	PME#	PME# from PCI slots.
GP 14	SMB Data Main	
GP 15	3V_SW_AUX	3V DUAL control
GP 16	WAKE#	PCI Express WAKE#, 1K PU to +3.3 V SB
GP 17	SMB_CLK_M	SMBus clock main
GP 21	DIAG_BEEP	Diagnostic beep signal; route to internal speaker amplifier
GP 22	CPUFAN_PWM	CPU Fan PWM command input, install 1K PU to +3.3 V
GP 23	AUDIO_AMP_DIS#	To disable internal speaker.

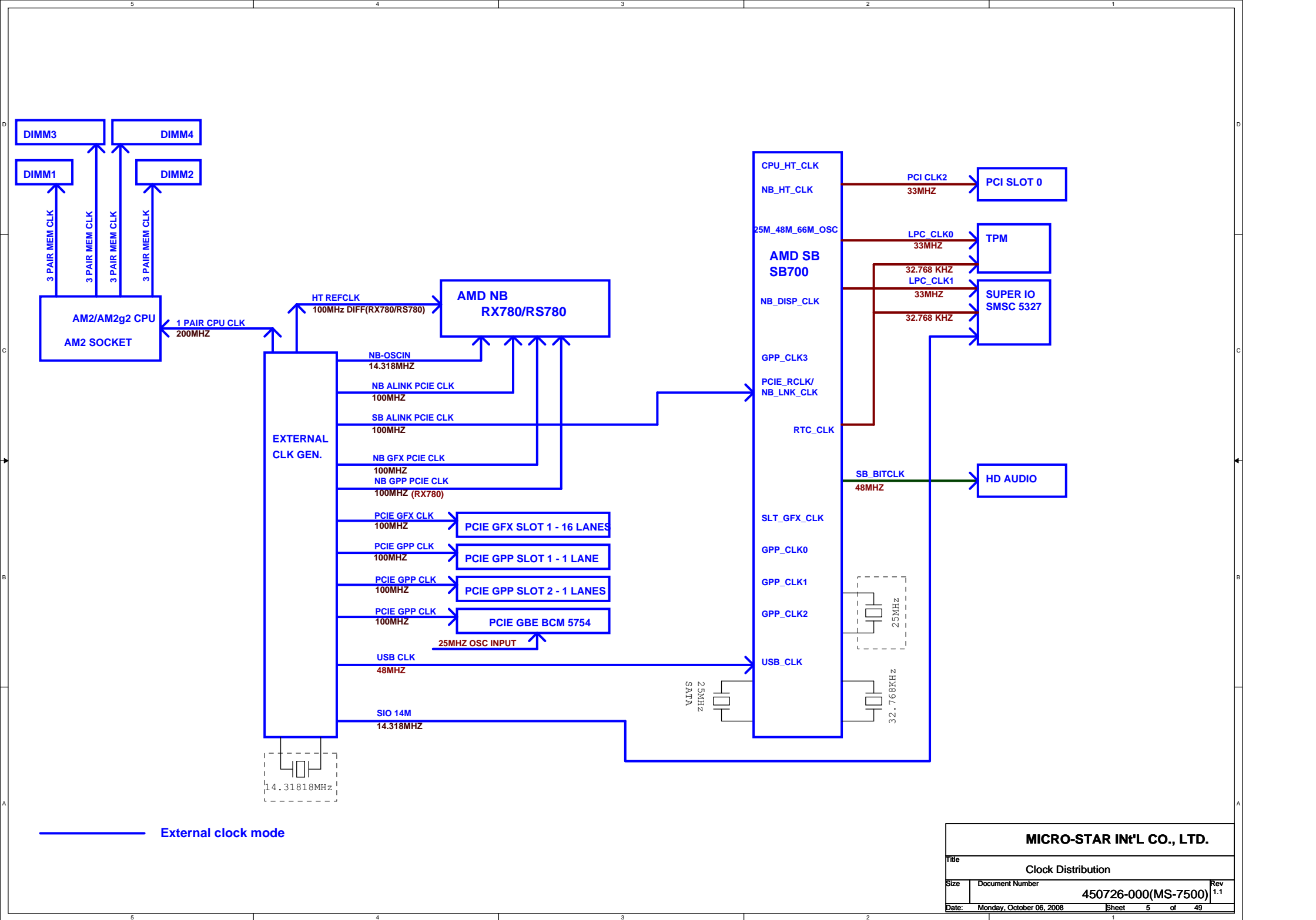
SIO GPIO	Function	Comment
GP 24	HOOD_SW_DET	Intrusion Switch Detect. Route to P126-1. Add 3.2K pullup to +3.3 V.
GP 25	HOOD_SENSE#	1M PU to SIO_BATT
GP 26	SKTOCC#	Route to SKTOCC# on CPU, install 10M PU to BATT, CPU occupied signal
GP 27	WAKE_OUT#	Wake Disable Output.
GP 30	LED_COLOR	Route to P5.4, front LED/button header, power LED driver
GP 31	LED_BLINK	Route to P5.2, front LED/button header, power LED driver
GP 32	TRMTRIP#	Route to Thermtrip# voltage translation, 8.2K PU to +3.3 V, CPU shutdown
GP 33	HD_LED_IN#	Route to Hard Drive LED control circuit.
GP 36	SMBCLK_THERM	SMB clock for sensor bus for fan sense chip; 4.7K PU to +3.3 V SB
GP 37	SMBDATA_THERM	SMB data for sensor bus for fan sense chip; 4.7K PU to +3.3 V SB
GP 40	DENSEL#	Route to P10.2, floppy connector
GP 41	HD_LED_OUT#	Hard drive LED output
GP 42	RING#	Power management output to Southbridge RING# input, 8.2K PU to +3.3 V SB
GP 43	SMB_CLK_R	SMBus clock resume
GP 44	HOOD_LOCK#	Route to P424-1, install 2.2K pullup to +3.3 V
GP 45	HOOD_UNLOCK#	Route to P424-6, install 2.2K pullup to +3.3 V
GP 46	LPC_SMI#	LPC SMI output to Southbridge, install 8.2K pull up to +3.3 V SB
GP 50	RIZ#	Route to 2 nd serial port RI# pin.
GP 51	DCD2#	Route to 2 nd serial port DCD# pin.
GP 52	RXD2#	Route to 2 nd serial port RxDAT pin.
GP 53	TXD2#	Route to 2 nd serial port TxDAT pin.
GP 54	DSR2#	Route to 2 nd serial port DSR# pin.
GP 55	RTS2#	Route to 2 nd serial port RTS# pin.
GP 56	CTS2#	Route to 2 nd serial port CTS# pin.
GP 57	DTR2#	Route to 2 nd serial port DTR# pin.
GP 60	CLAMP_CTRL	Clamp Control Signal. Route to power bleed off transistors.
GP 61	SIO_PCIE_RST#	Reset; route to PCI Express X1 and x16 slots
GP 62	PWRBTN_IN#	Front panel power button input
GP 63	SLP_S3#	Connected to S3 sleep input from Southbridge
GP 64	SLP_S5#	Connected to SLP_S5# sleep input from Southbridge
GP 66	PWRBTN_OUT#	Route to Southbridge PWRBTN# input
GP 67	PSON#	Power supply main voltage control; route to P1. 16, install 2.2K PU to +5 VAUX
GP 70	USB_PWR#	Connected to SLP_S5#
GP 71	SMB DATA Resume	
GP 72	5V_DUAL_Control	Controls aux voltage FET on 5V_DUAL circuit
GP 73	CHAFAN2_TACH	Power supply tach input; 4.7K PU to +3.3 V
GP 74	CHAFAN2_PWM	Power supply PWM command input; 1K PU to +3.3 V
GP 75	PWRGD_30MS	Power Good delayed 30 ms. 1K PU to +3 V SB
GP 76	PWRGD_50MS#	Inverted Power Good delayed 50 ms. 1K PU to +3 V SB
GP 85	CPUFAN_TACH	Tach input from CPU fan connector, 4.7K PU to +3.3 V

ATI SB700 GPIO Matrix

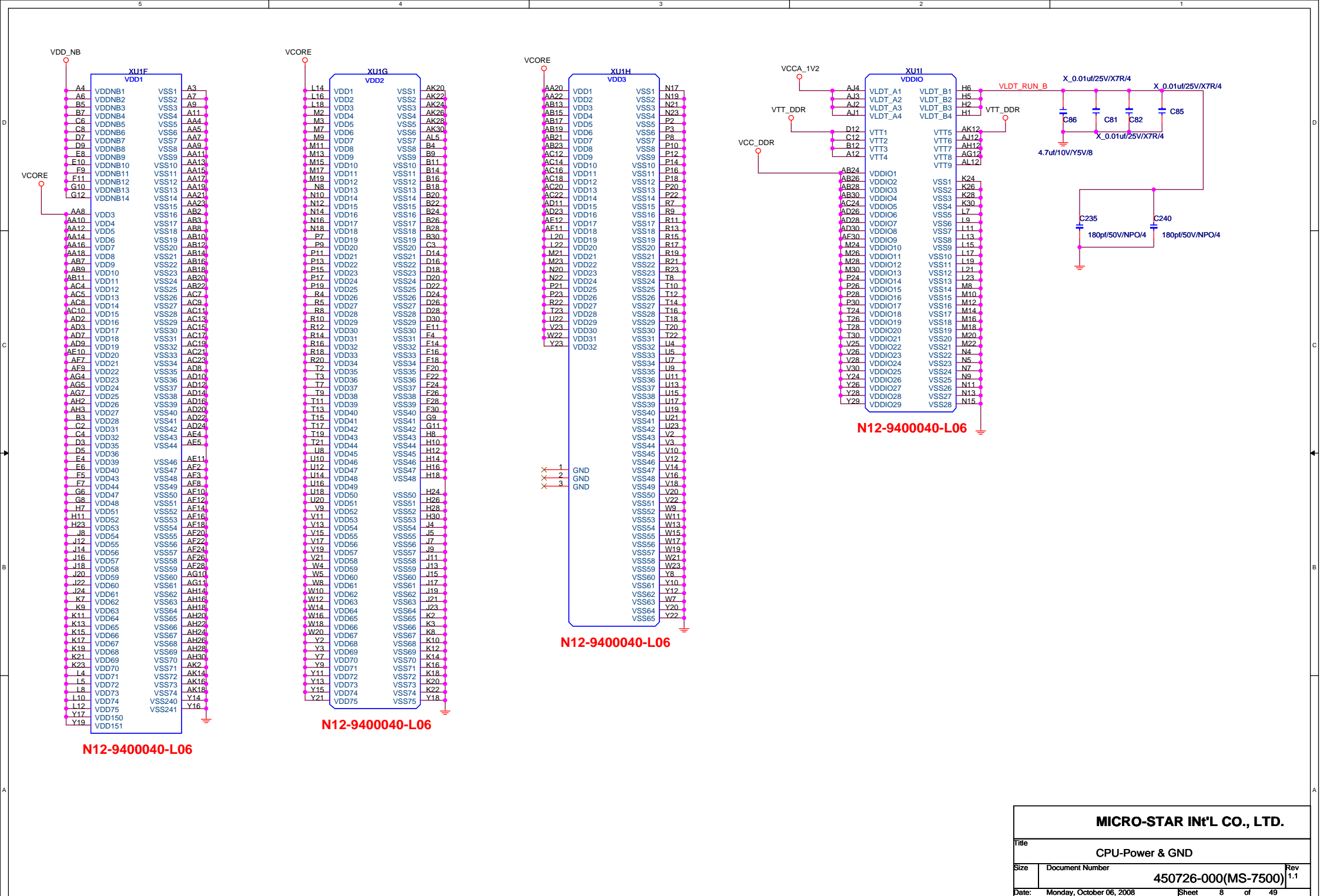
Pin Capabilities							Pin Defaults			BIOS Assignments				
Pin	GPIO	Alternate Functions	Strapping Function / Internal PU or PD	Input/Output	Power Well	Voltage Tolerance	Default Signal Definition	Default Buffer Type	Default Output Level	Function	Input/Output	Output Level	Motherboard Function	Implementation Notes
W17	GPIO 0	SSMUXSEL/SATA_IS3#		I/O	Vbc3_3	5				GPIO 0	I		BRD_ID0	
A26	GPIO 1	ROM_CS#		I/O	Vbc3_3	5		I		GPIO 1	I			
W21	GPIO 2	SPKR		I/O	Vbc3_3	5				SPKR	O		SB800 SPKR_OUT	
M6	GPIO 3	FANOUT0		I/O	Vbc3_3	5		I		GPIO 3	I		PROCHOT2_SB	
AA19	GPIO 4	SMARTVOLT/SATA_IS2#		I/O	Vbc3_3	5		TRI-STATE		GPIO 4	I		BRD_REV0	
Y19	GPIO 5	SHUTDOWN#		I/O	Vbc3_3	5		TRI-STATE		GPIO 5	I		BRD_REV1	
AD18	GPIO 6	GHM/SATA_IS1#		I/O	Vbc3_3	5		TRI-STATE		GPIO 6	I		CHASSIS_ID0	
A23	GPIO 7	WD_PWRGD		I/O	Vbc3_3	5		TRI-STATE		GPIO 7	I			
Y18	GPIO 8	DDC1_SDA		I/O	Vbc3_3	5		TRI-STATE		GPIO 8	I		CHASSIS_ID2	
AA20	GPIO 9	DDC1_SCL		I/O	Vbc3_3	5		TRI-STATE		GPIO 9	I		BRD_ID1	
AE18	GPIO 10	SATA_IS0#		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 10	I	3.3_ID1	CHASSIS_ID1	
D2	GPIO 11	SPI_D0		I/O	Vbc3_3	3.3		TRI-STATE		SPI_D0	O		SPI_DATA_OUT	
G6	GPIO 12	SPI_D1		I/O	Vbc3_3	3.3		TRI-STATE		SPI_D1	I		SPI_DATA_IN	
U16	GPIO 13	LAN_RST#		OD	Vbc3_3	5			0					
GPIO 14	ROM_RST#			I/O	Vbc3_3	5			0	ROM_RST#	O			
AD24	GPIO 15	IDE_D0		I/O	Vbc3_3	5		TRI-STATE		IDE_D0	I/O			
AD23	GPIO 16	IDE_D1		I/O	Vbc3_3	5		TRI-STATE		IDE_D1	I/O			
AE22	GPIO 17	IDE_D2		I/O	Vbc3_3	5		TRI-STATE		IDE_D2	I/O			
AC22	GPIO 18	IDE_D3		I/O	Vbc3_3	5		TRI-STATE		IDE_D3	I/O			
AD21	GPIO 19	IDE_D4		I/O	Vbc3_3	5		TRI-STATE		IDE_D4	I/O			
AE20	GPIO 20	IDE_D5		I/O	Vbc3_3	5		TRI-STATE		IDE_D5	I/O			
AD20	GPIO 21	IDE_D6		I/O	Vbc3_3	5		TRI-STATE		IDE_D6	I/O			
AD19	GPIO 22	IDE_D7		I/O	Vbc3_3	5		TRI-STATE		IDE_D7	I/O			
AE19	GPIO 23	IDE_D8		I/O	Vbc3_3	5		TRI-STATE		IDE_D8	I/O			
AC20	GPIO 24	IDE_D9		I/O	Vbc3_3	5		TRI-STATE		IDE_D9	I/O			
AD20	GPIO 25	IDE_D10		I/O	Vbc3_3	5		TRI-STATE		IDE_D10	I/O			
AE21	GPIO 26	IDE_D11		I/O	Vbc3_3	5		TRI-STATE		IDE_D11	I/O			
AB22	GPIO 27	IDE_D12		I/O	Vbc3_3	5		TRI-STATE		IDE_D12	I/O			
AD22	GPIO 28	IDE_D13		I/O	Vbc3_3	5		TRI-STATE		IDE_D13	I/O			
AE23	GPIO 29	IDE_D14		I/O	Vbc3_3	5		TRI-STATE		IDE_D14	I/O			
AC23	GPIO 30	IDE_D15		I/O	Vbc3_3	5		TRI-STATE		IDE_D15	I/O			
F4	GPIO 31	SPI_HOLD#		I/O	Vbc3_3	3.3		TRI-STATE		SPI_HOLD	O		SPI_HOLD#	
F3	GPIO 32	SPI_CS#		I/O	Vbc3_3	3.3		TRI-STATE		SPI_CS#	O		SPI_CHIP_SELECT#	
AD3	GPIO 33	INT#		I/O	Vbc3_3	5		TRI-STATE		INT#			PCI_INT#	To PCI slots J21 & J22.
AC4	GPIO 34	INT#		I/O	Vbc3_3	5		TRI-STATE		INT#			PCI_INT#	To PCI slots J21 & J22.
AE2	GPIO 35	INT#		I/O	Vbc3_3	5		TRI-STATE		INT#			PCI_INT#	To PCI slots J21 & J22.
AE3	GPIO 36	INT#		I/O	Vbc3_3	5		TRI-STATE		INT#			PCI_INT#	To PCI slots J21 & J22.
B24	GPIO 37	DRSLP_ODM#	Open drain. Requires external pullup to Vbc3_3.	I/O	Vbc3_3	5		TRI-STATE						
LL	GPIO 38	AC_BTCLK	STRAP: Not enable debug chip, low-voltage hysteresis enabled.	I/O	Vbc3_3	5		I						
V17	GPIO 39	AC_SDOUT		I/O	Vbc3_3	5		0						
W20	GPIO 40	CLK_REQ2/SATA_IS6		I/O	Vbc3_3	5		I						
T3	GPIO 41	PCICLK5		I/O	Vbc3_3	5								
J7	GPIO 42	AC_SDIN0		I/O	Vbc3_3	3.3		I						
J8	GPIO 43	AC_SDIN1		I/O	Vbc3_3	3.3		I						
L8	GPIO 44	AC_SDIN2		I/O	Vbc3_3	3.3		I						
LC	GPIO 45	AC_RST#		I/O	Vbc3_3	3.3		0						
M0	GPIO 46	AC_SDIN3		I/O	Vbc3_3	3.3				AC2 SDIN	I		AZALIA AUDIO IN 0	
D1	GPIO 47	SPI_CLK		I/O	Vbc3_3	3.3				SPI_CLK	O		SPI_CLOCK	
M5	GPIO 48	FANOUT1		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 48	I		COMMA_B_DET#	
M7	GPIO 49	FANOUT2		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 49	I		FRONT_AUD_DET#	
P5	GPIO 50	FANIN0		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 50	I		FRONT_USB_DET#	
P8	GPIO 51	FANIN1		I/O	Vbc3_3	3.3		TRI-STATE						
R8	GPIO 52	FANIN2		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 52	I		PASSWORD_ENABLE	
AA	GPIO 53	VIN0		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 53	I		BOOT_BLOCK_ENABLE	
B4	GPIO 54	VIN1		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 54	I		BOOT_BLOCK_RECOVER	
C4	GPIO 55	VIN2		I/O	Vbc3_3	3.3		TRI-STATE		GPIO 55	I		BRD_ID2	
D5	GPIO 56	VIN3		I/O	Vbc3_3	3.3		TRI-STATE						
D6	GPIO 57	VIN4		I/O	Vbc3_3	3.3		TRI-STATE						
D8	GPIO 58	VIN5		I/O	Vbc3_3	3.3		TRI-STATE						
A7	GPIO 59	VIN6		I/O	Vbc3_3	3.3		TRI-STATE						
B7	GPIO 60	VIN7		I/O	Vbc3_3	3.3		TRI-STATE						
B6	GPIO 61	TEMPIN0		I/O	Vbc3_3	3.3		TRI-STATE						
A6	GPIO 62	TEMPIN1		I/O	Vbc3_3	3.3		TRI-STATE						
A5	GPIO 63	TEMPIN2		I/O	Vbc3_3	3.3		TRI-STATE						
B5	GPIO 64	TEMPIN3/ALERT#		I/O	Vbc3_3	3.3		TRI-STATE						
AD7	GPIO 65	BMREQ/REQ0#		I/O	Vbc3_3	3.3		TRI-STATE						
C1	GPIO 66	LLB#		I/O	Vbc3_3	3.3		TRI-STATE						
W11	GPIO 67	SATA_ACT#		I/O	Vbc3_3	3.3		TRI-STATE		SATA_ACT	O		SATA_LED_SB	
AB8	GPIO 68	LDR01#/GN15#		I/O	Vbc3_3	5		TRI-STATE						
F5	GPIO 69	RTC_IRQ#		I/O	3V6BAT	3.3		0						
AB5	GPIO 70	REQ3#		I/O	Vbc3_3	5		TRI-STATE						
AB6	GPIO 71	REQ4#		I/O	Vbc3_3	5		TRI-STATE		GPIO 71	I		PRT_DET#	
AC6	GPIO 72	GN13#		I/O	Vbc3_3	5		0						
AE5	GPIO 73	GN14#		I/O	Vbc3_3	5		0						

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Title			GPIO Table
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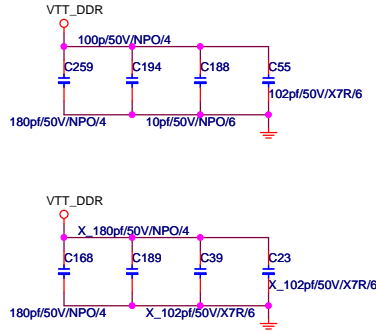




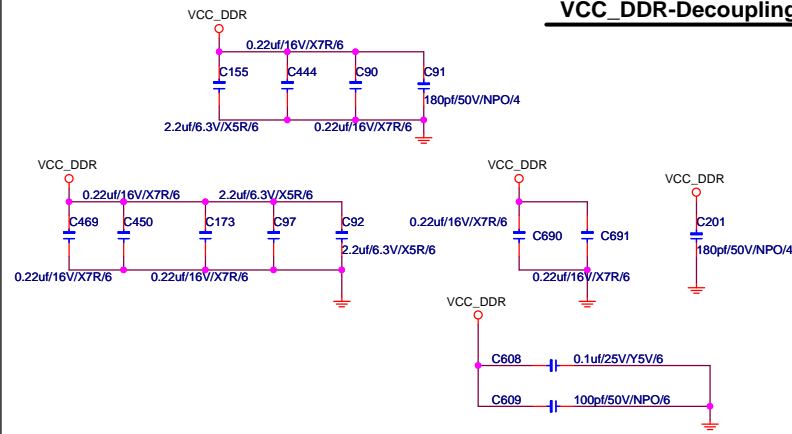
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Title		CPU-Power & GND	
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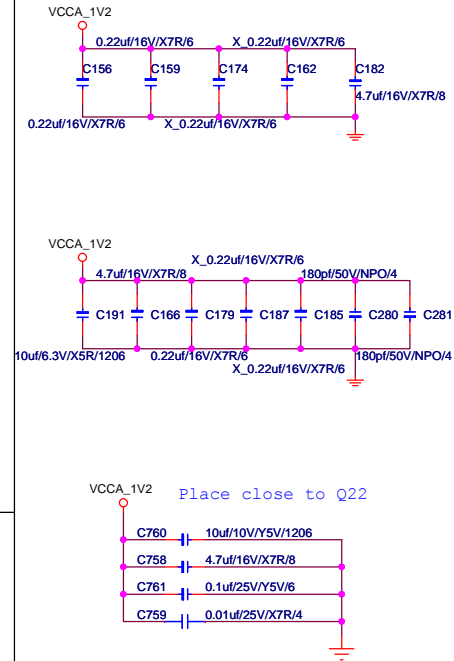
VTT_DDR-Decoupling



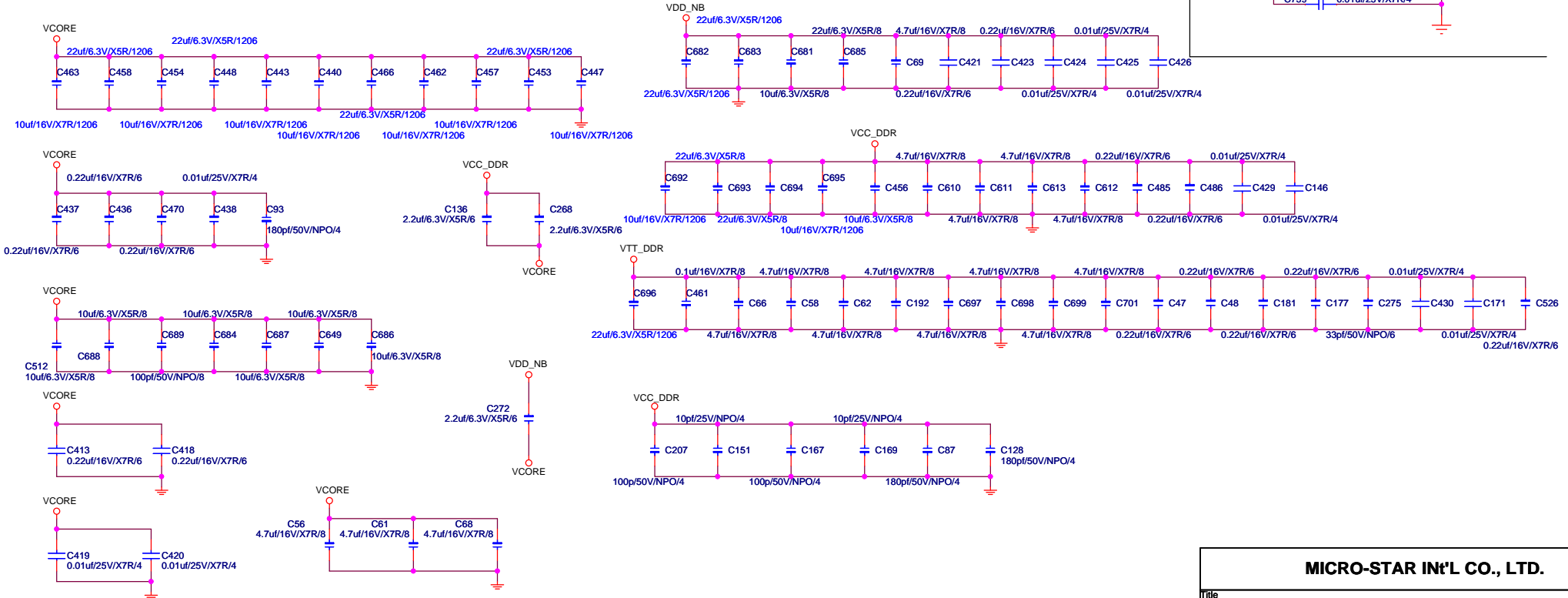
VCC_DDR-Decoupling



VCCA_1V2-Decoupling

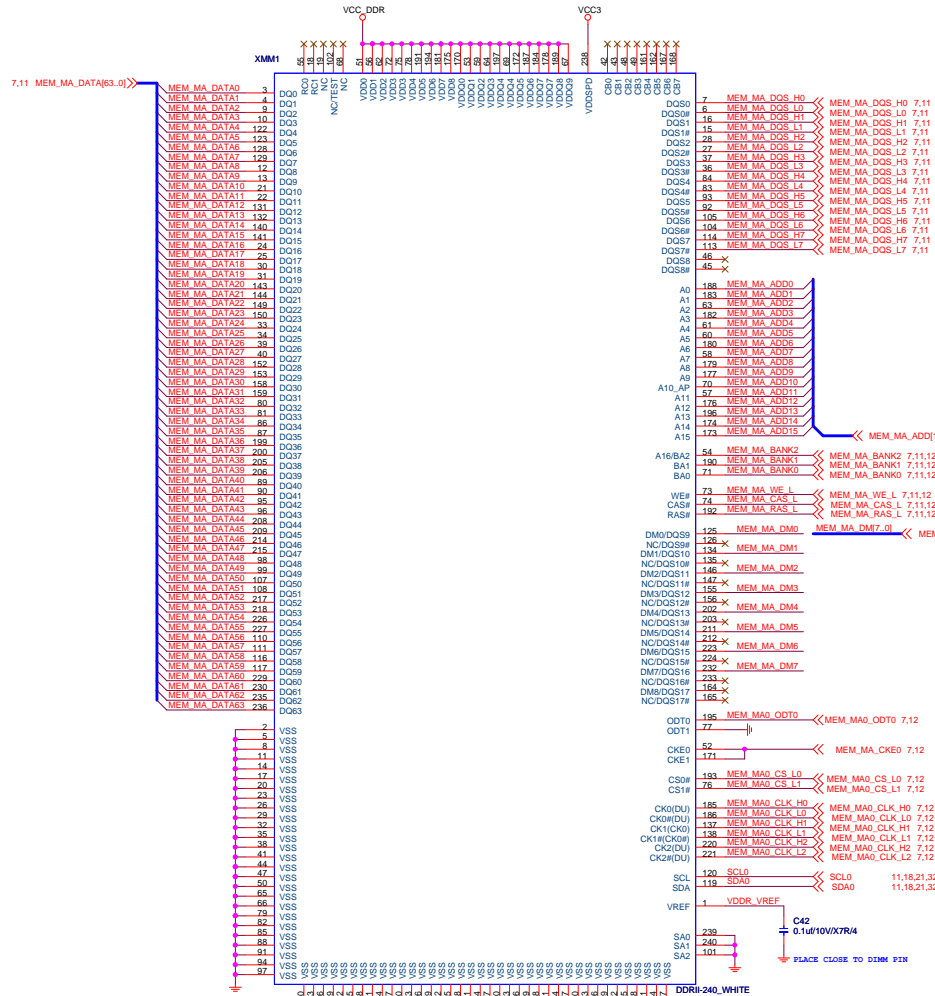


VCORE-Decoupling



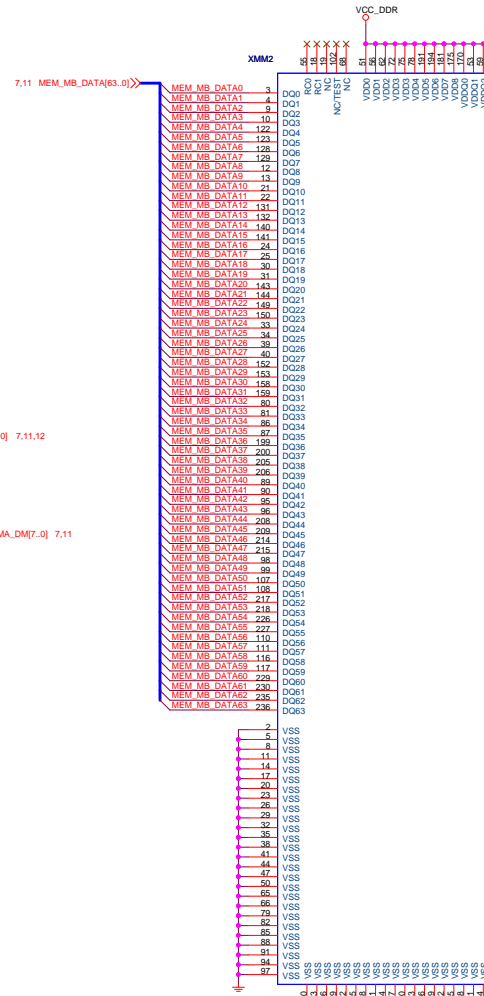
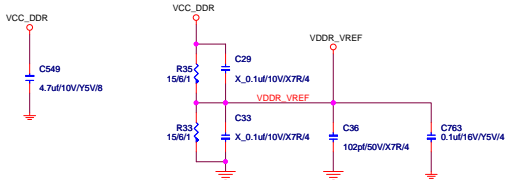
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Title			CPU-Decoupling
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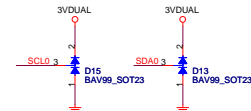
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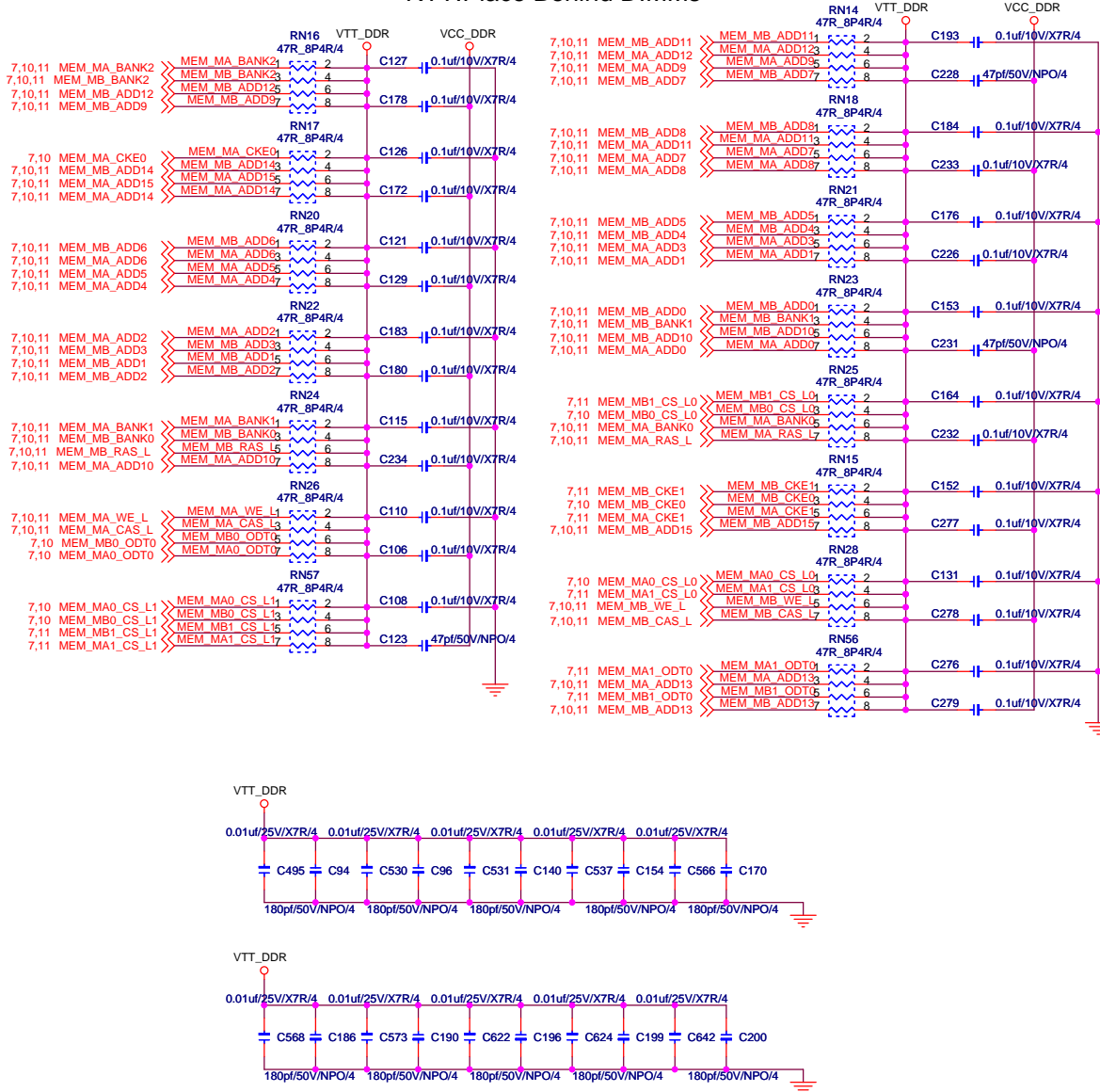


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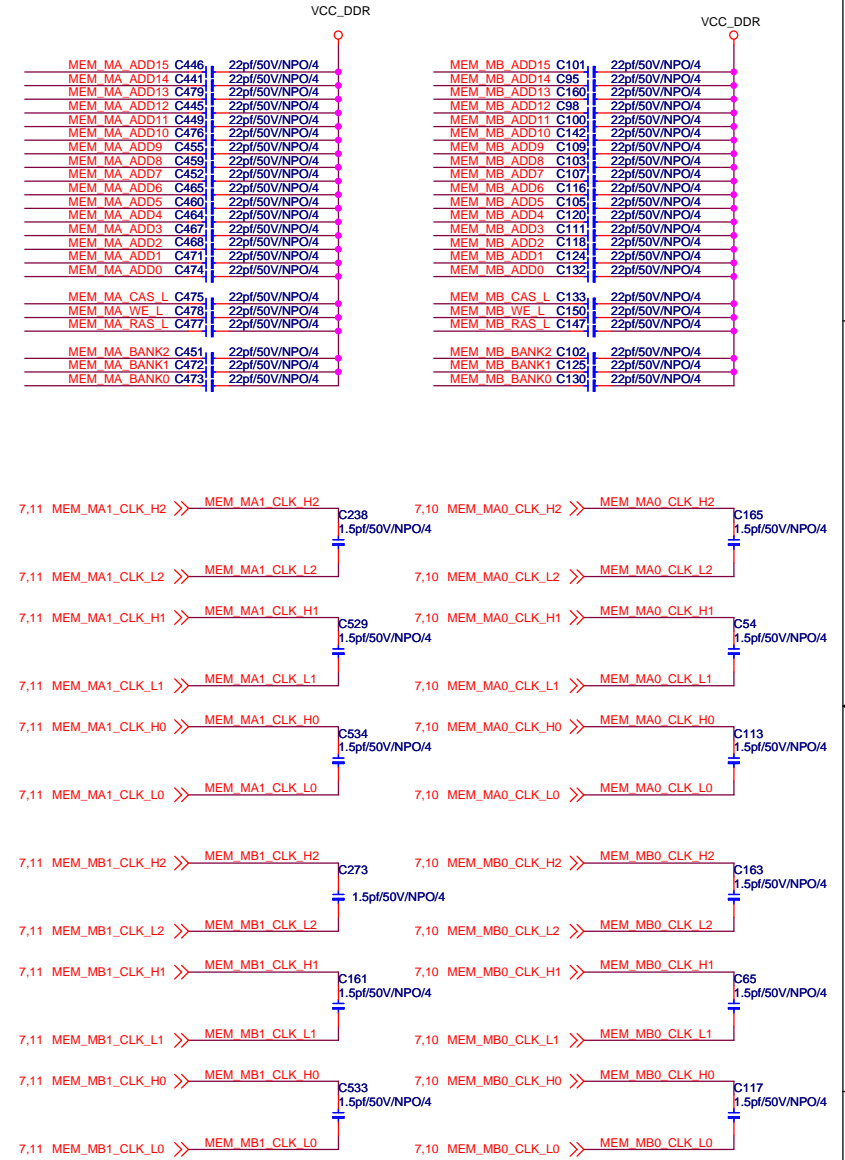
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RTT:Place Behind DIMMs



Place Between Processor and DIMMs



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Title			
DDR II Termination			
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6 CADOP[0..15] >> CADOP[0..15]

6 CADON[0..15] >> CADON[0..15]

20 / 5 / 5 / 5 / 20

CADOP0 Y25 HT_RXCAD0P
CADON0 Y24 HT_RXCAD0N
CADOP1 V22 HT_RXCAD1P
CADON1 V23 HT_RXCAD1N
CADOP2 V25 HT_RXCAD2P
CADON2 V24 HT_RXCAD2N
CADOP3 U24 HT_RXCAD3P
CADON3 U25 HT_RXCAD3N
CADOP4 T25 HT_RXCAD4P
CADON4 T24 HT_RXCAD4N
CADOP5 P22 HT_RXCAD5P
CADON5 P23 HT_RXCAD5N
CADOP6 P25 HT_RXCAD6P
CADON6 P24 HT_RXCAD6N
CADOP7 N24 HT_RXCAD7P
CADON7 N25 HT_RXCAD7N

CADOP8 AC24 HT_RXCAD8P
CADON8 AC25 HT_RXCAD8N
CADOP9 AB24 HT_RXCAD9P
CADON9 AB25 HT_RXCAD9N
CADOP10 AA24 HT_RXCAD10P
CADON10 AA25 HT_RXCAD10N
CADOP11 Y22 HT_RXCAD11P
CADON11 Y23 HT_RXCAD11N
CADOP12 W21 HT_RXCAD12P
CADON12 W20 HT_RXCAD12N
CADOP13 V21 HT_RXCAD13P
CADON13 V20 HT_RXCAD13N
CADOP14 U20 HT_RXCAD14P
CADON14 U21 HT_RXCAD14N
CADOP15 U19 HT_RXCAD15P
CADON15 U18 HT_RXCAD15N

6 CLKOP0 >> CLKOP0 T22 HT_RXCLK0P
6 CLKON0 >> CLKON0 T23 HT_RXCLK0N
6 CLKOP1 >> CLKOP1 AB23 HT_RXCLK1P
6 CLKON1 >> CLKON1 AA22 HT_RXCLK1N

6 CTLOP0 >> CTLOP0 M22 HT_RXCTL0P
6 CTLOP1 >> CTLOP1 M23 HT_RXCTL0N
6 CTLOP2 >> CTLOP2 R21 HT_RXCTL1P
6 CTLOP3 >> CTLOP3 R20 HT_RXCTL1N

301/4/1 R34 HT_RXCALP C23 HT_RXCALP
HT_RXCALN A24 HT_RXCALN

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PART 1 OF 6

HYPER TRANSPORT CPU
I/F

HT_TXCAD0P D24 CADIP0
HT_TXCAD0N D25 CADIN0
HT_TXCAD1P E24 CADIP1
HT_TXCAD1N E25 CADIN1
HT_TXCAD2P F24 CADIP2
HT_TXCAD2N F25 CADIN2
HT_TXCAD3P F23 CADIP3
HT_TXCAD3N F22 CADIN3
HT_TXCAD4P H23 CADIP4
HT_TXCAD4N H22 CADIN4
HT_TXCAD5P J25 CADIP5
HT_TXCAD5N J24 CADIN5
HT_TXCAD6P K24 CADIP6
HT_TXCAD6N K25 CADIN6
HT_TXCAD7P K23 CADIP7
HT_TXCAD7N K22 CADIN7

HT_TXCAD8P G21 CADIP8
HT_TXCAD8N G20 CADIN8
HT_TXCAD9P H21 CADIP9
HT_TXCAD9N H20 CADIN9
HT_TXCAD10P J21 CADIP10
HT_TXCAD10N J18 CADIN10
HT_TXCAD11P K17 CADIP11
HT_TXCAD11N L19 CADIN11
HT_TXCAD12P L18 CADIP12
HT_TXCAD12N M19 CADIN12
HT_TXCAD13P L18 CADIP13
HT_TXCAD13N M21 CADIN13
HT_TXCAD14P P21 CADIP14
HT_TXCAD14N P18 CADIN14
HT_TXCAD15P P18 CADIP15
HT_TXCAD15N M18 CADIN15

H24 CLKIP0 >> CLKIP0 6
H25 CLKIN0 >> CLKIN0 6
L21 CLKIP1 >> CLKIP1 6
L20 CLKIN1 >> CLKIN1 6

M24 CTLIPO >> CTLIPO 6
M25 CTLIN0 >> CTLIN0 6
P19 CTLIP1 >> CTLIP1 6
P18 CTLIN1 >> CTLIN1 6

B24 HT_TXCALP R36 301/4/1
B25 HT_TXCALN

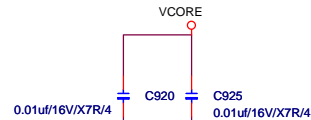
5 / 10

CADIP[0..15] >> CADIP[0..15] 6

CADIN[0..15] >> CADIN[0..15] 6

RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			



Adding some 0.01 μ F stitching capacitors for crossing a split when these signals change different reference layer.

For 07/09/07

08/10/07 AMD: Please note that R34 and R36 are 301 1% resistor when using RS780.

R34 and R36 are 1.21K 1% resistor when using RX780.

MICRO-STAR IN'L CO., LTD.

Title

RS780/RX780-HT LINK I/F

Size

Document Number

Date

Monday, October 06, 2008

Sheet

13

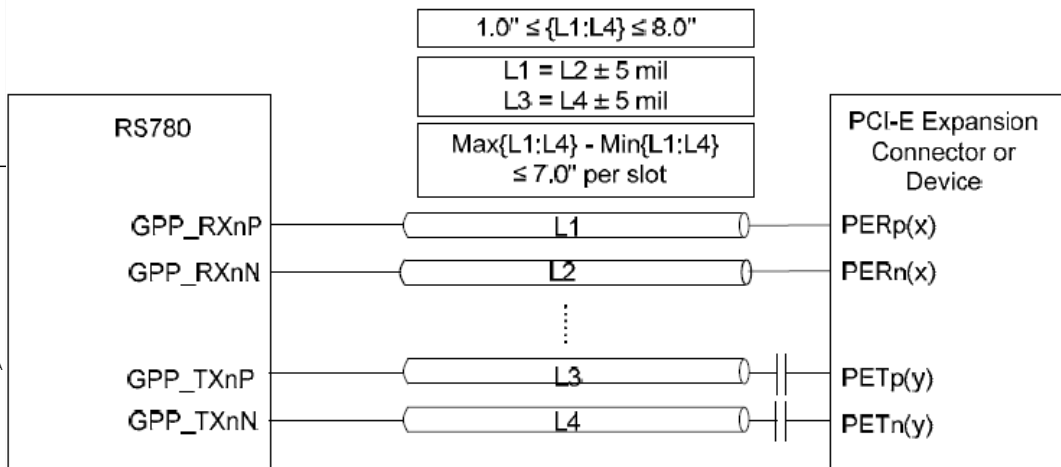
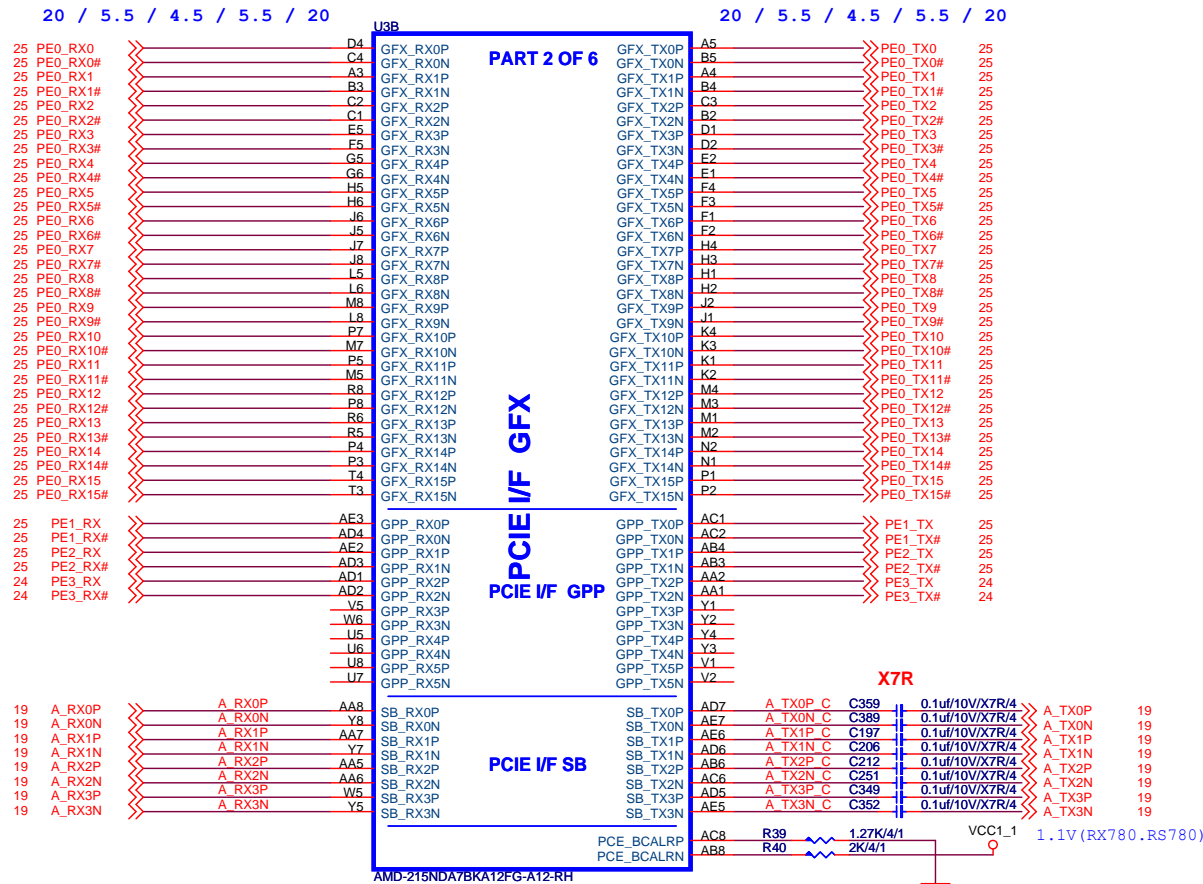
of

49

Rev

1.1

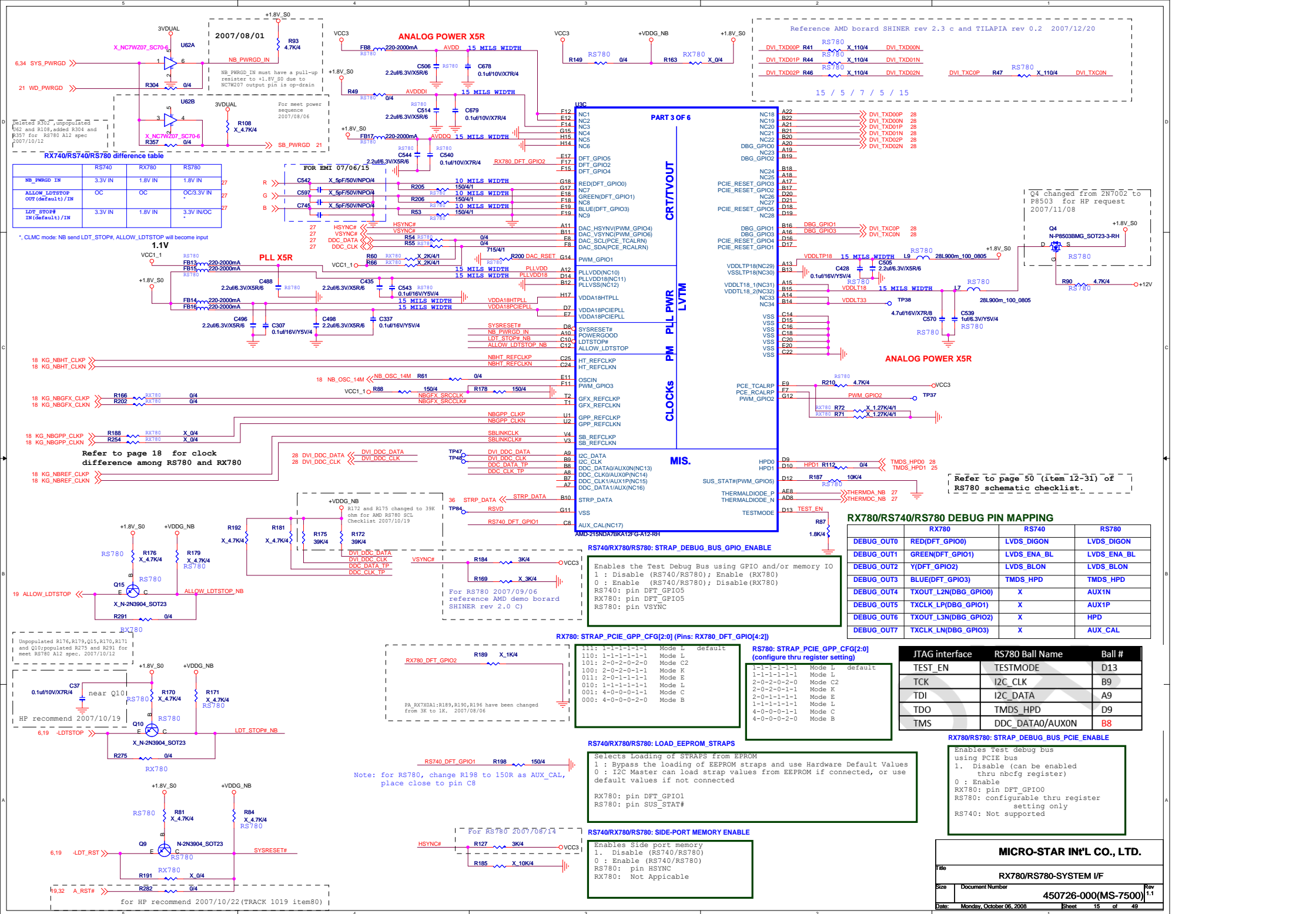
450726-000(MS-7500)

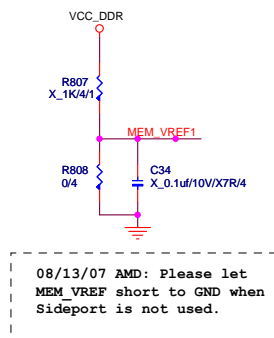
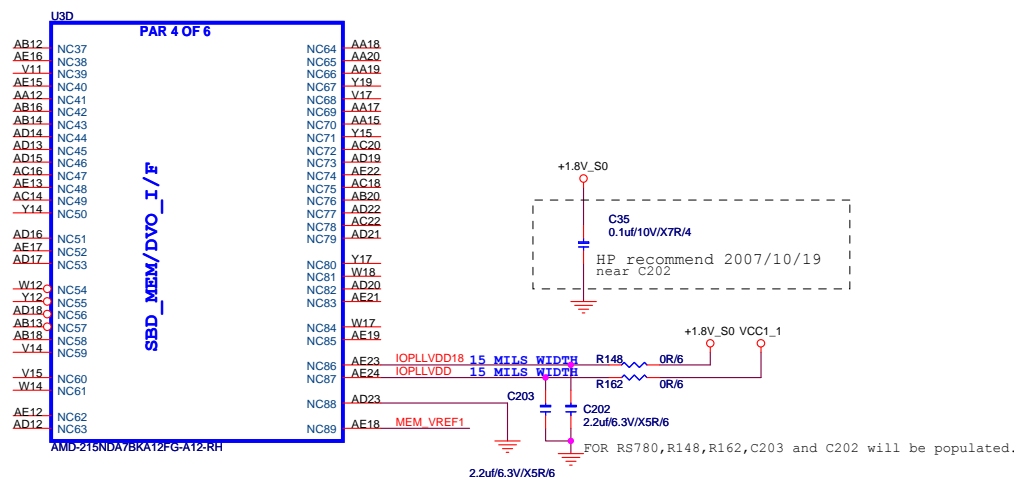


RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

Figure 39: Layout Guidelines for the PCI-Express Expansion Interface

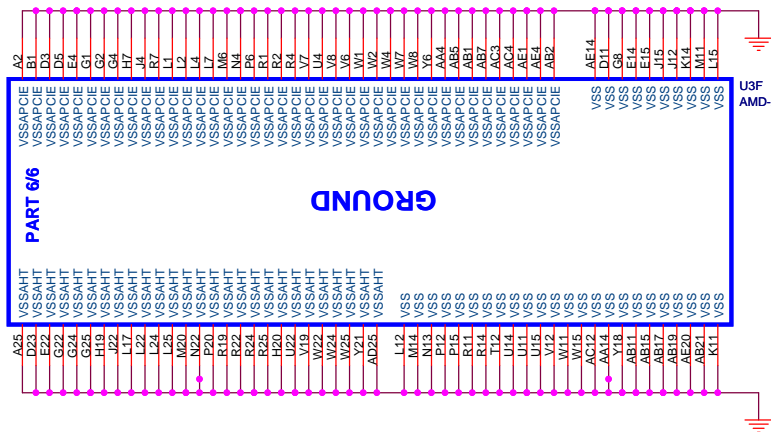




Note: If the Side-port memory interface is **not** used, make sure that:

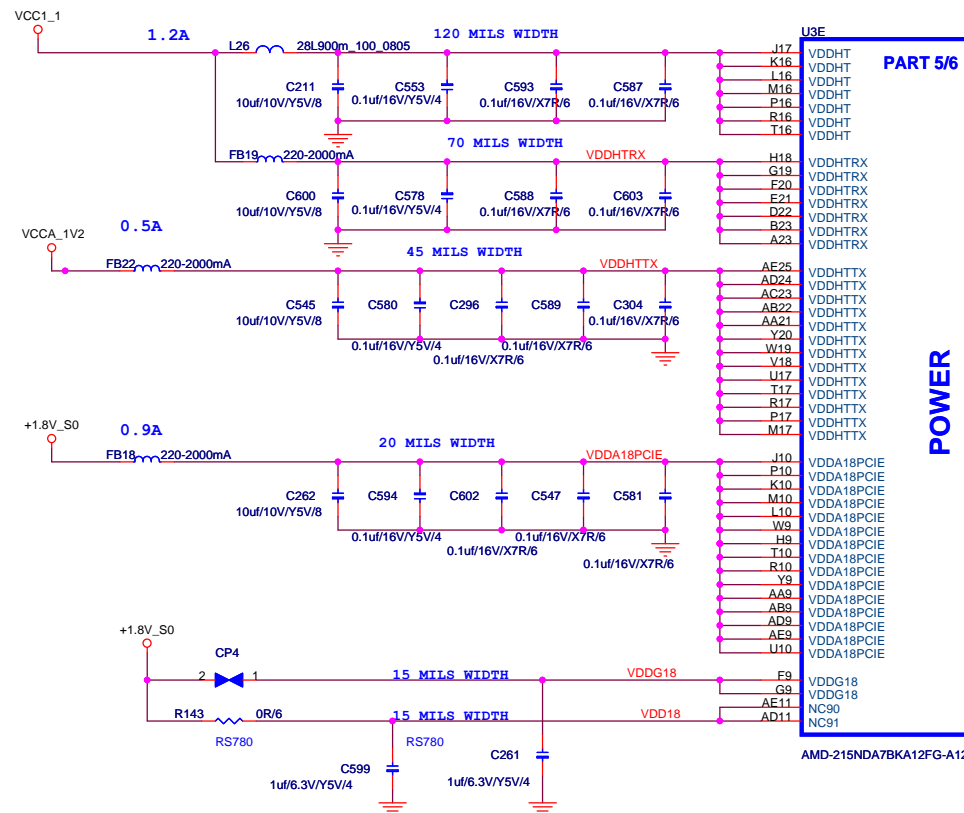
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

MICRO-STAR INT'L CO., LTD.			
Title			
SPMEM/STRAPS			
Size	Document Number	450726-000(MS-7500)	Rev 1.1
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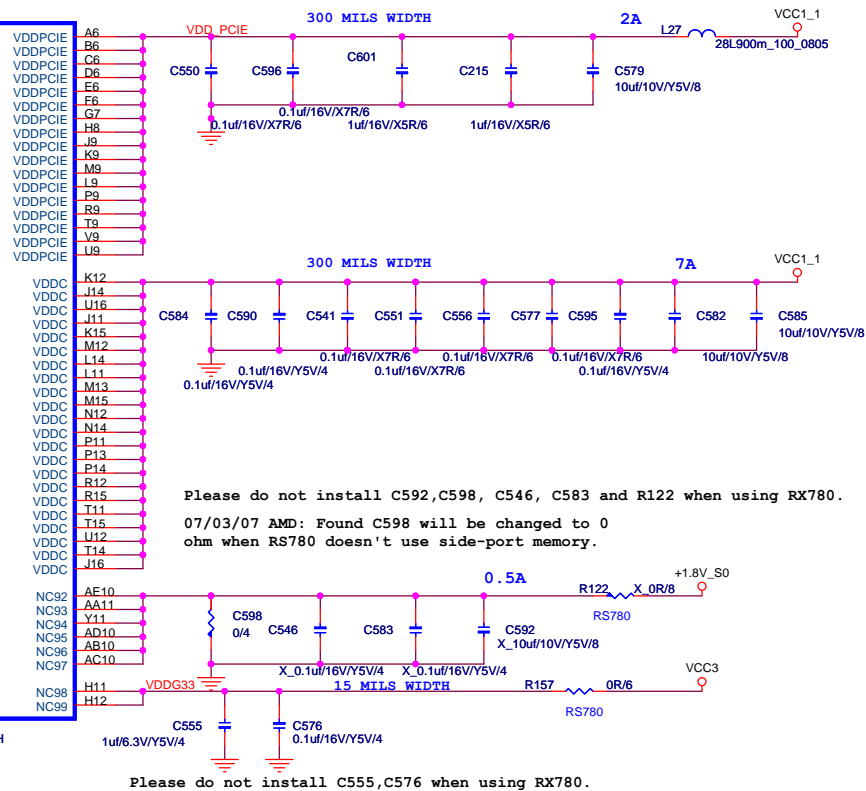


RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



POWER



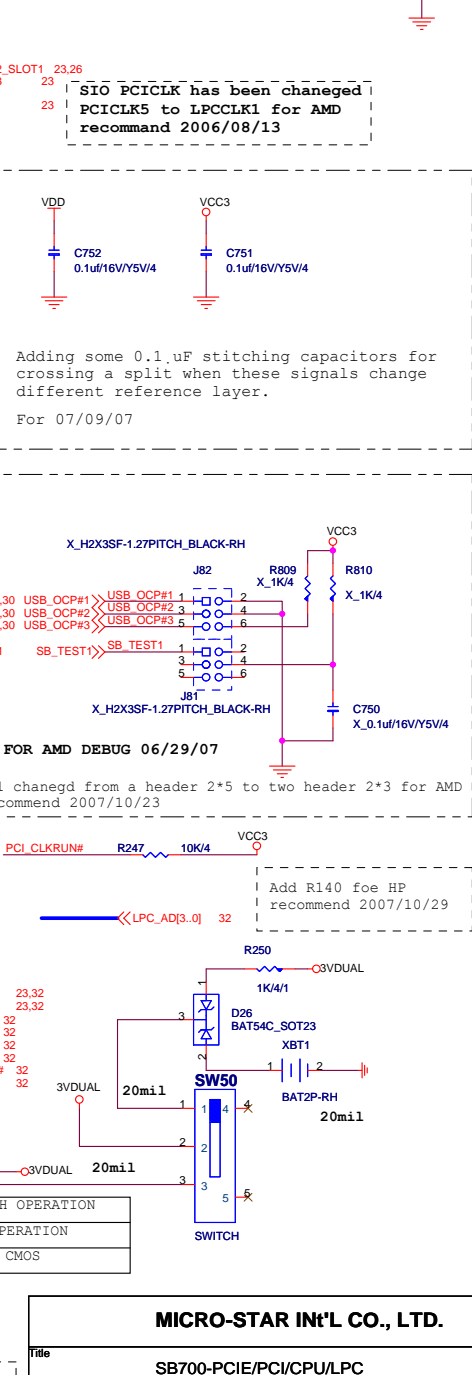
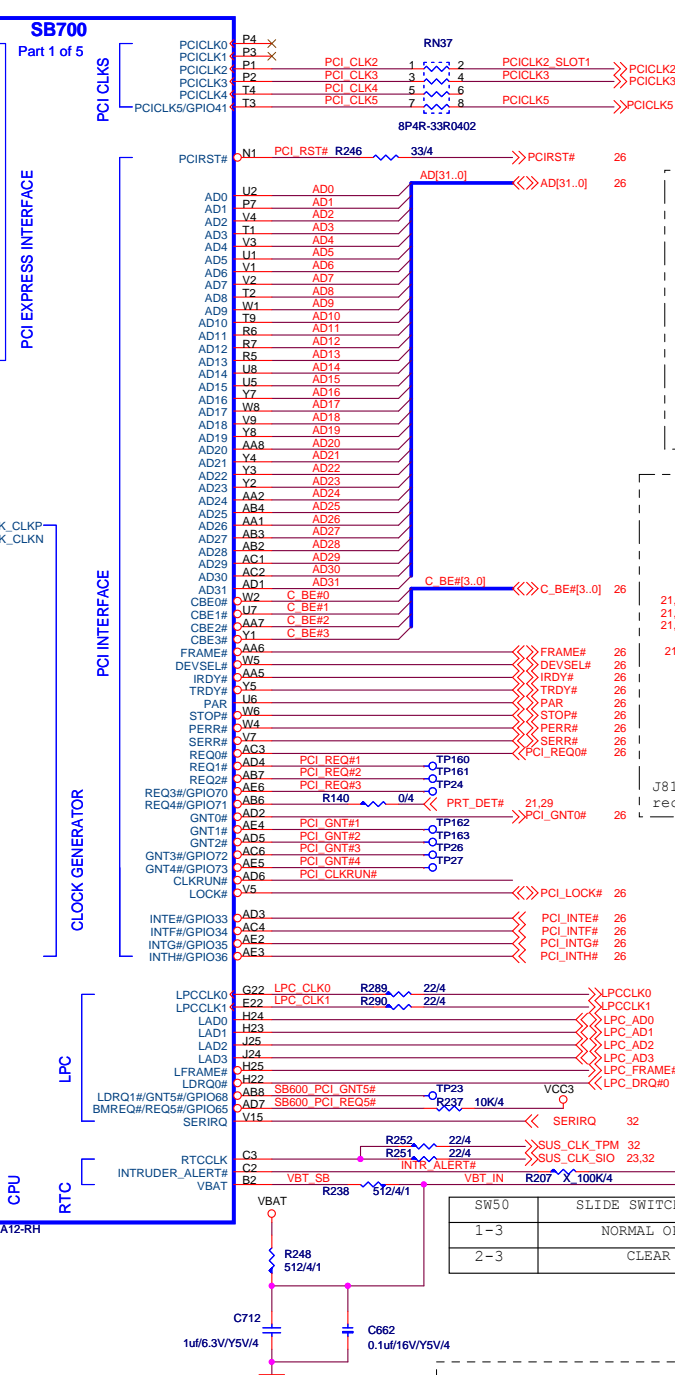
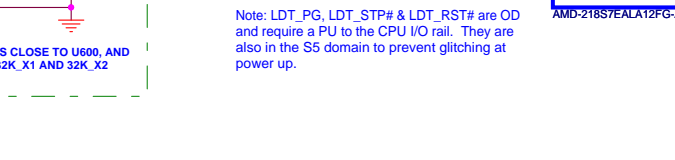
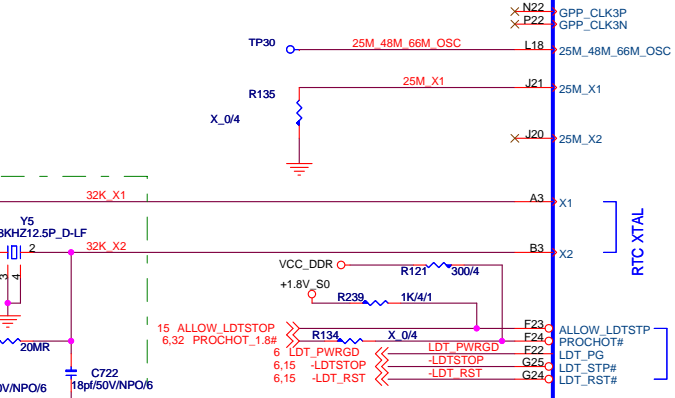
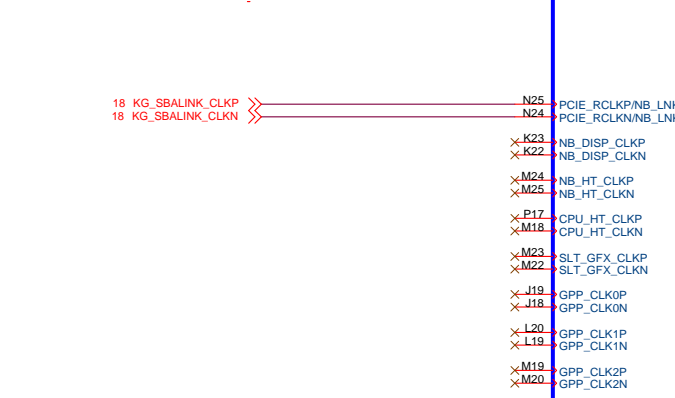
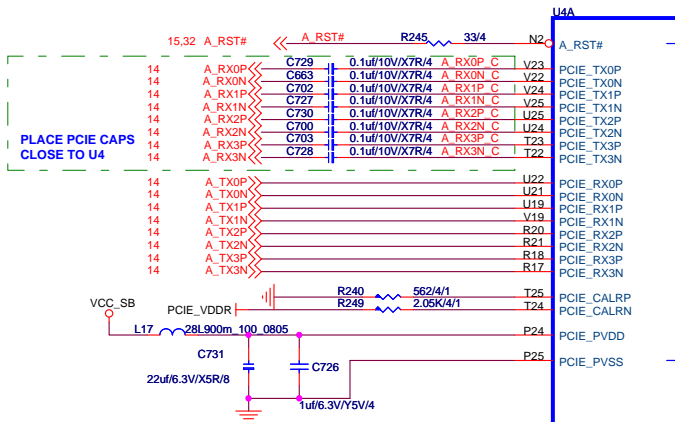
Please do not install C592, C598, C546, C583 and R122 when using RX780.
07/03/07 AMD: Found C598 will be changed to 0 ohm when RS780 doesn't use side-port memory.

Please do not install C555, C576 when using RX780.

07/03/07 AMD: Found C599 will be changed to 0 ohm when RS780 doesn't use side-port memory.
08/26/07 AMD: recommend R143 install 0 ohm and C599 install 1uf.

MICRO-STAR IN'L CO., LTD.

Title			RX780/RS780-POWER	
Size	Document Number		450726-000(MS-7500)	
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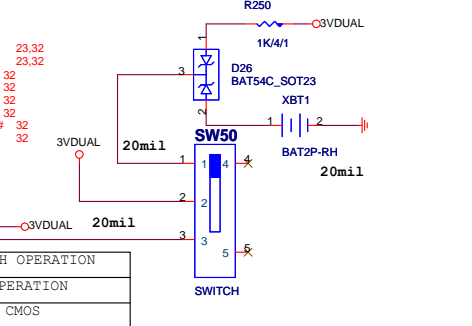
For EMI
PCICLK2 SLOT1 C725 15pF/50V/NPO/4
PCICLK3 C716 15pF/50V/NPO/4
PCICLK5 C718 15pF/50V/NPO/4

SIO PCICLK has been changed
PCICLK5 to LPCCLK1 for AMD
recommnd 2006/08/13

VDD C752 0.1uF/16V/Y5V/4
VCC3 C751 0.1uF/16V/Y5V/4
Adding some 0.1uF stitching capacitors for
crossing a split when these signals change
different reference layer.
For 07/09/07

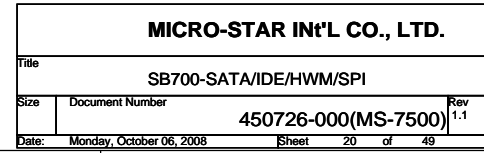
X_H2X3SF-1.27PITCH_BLACK-RH
J82 X_1K/4
R809 X_1K/4
R810 X_1K/4
C750 X_0.1uF/16V/Y5V/4
21 SB_TEST1 SB TEST1
FOR AMD DEBUG 06/29/07
J81 chanegd from a header 2*5 to two header 2*3 for AMD
recommnd 2007/10/23

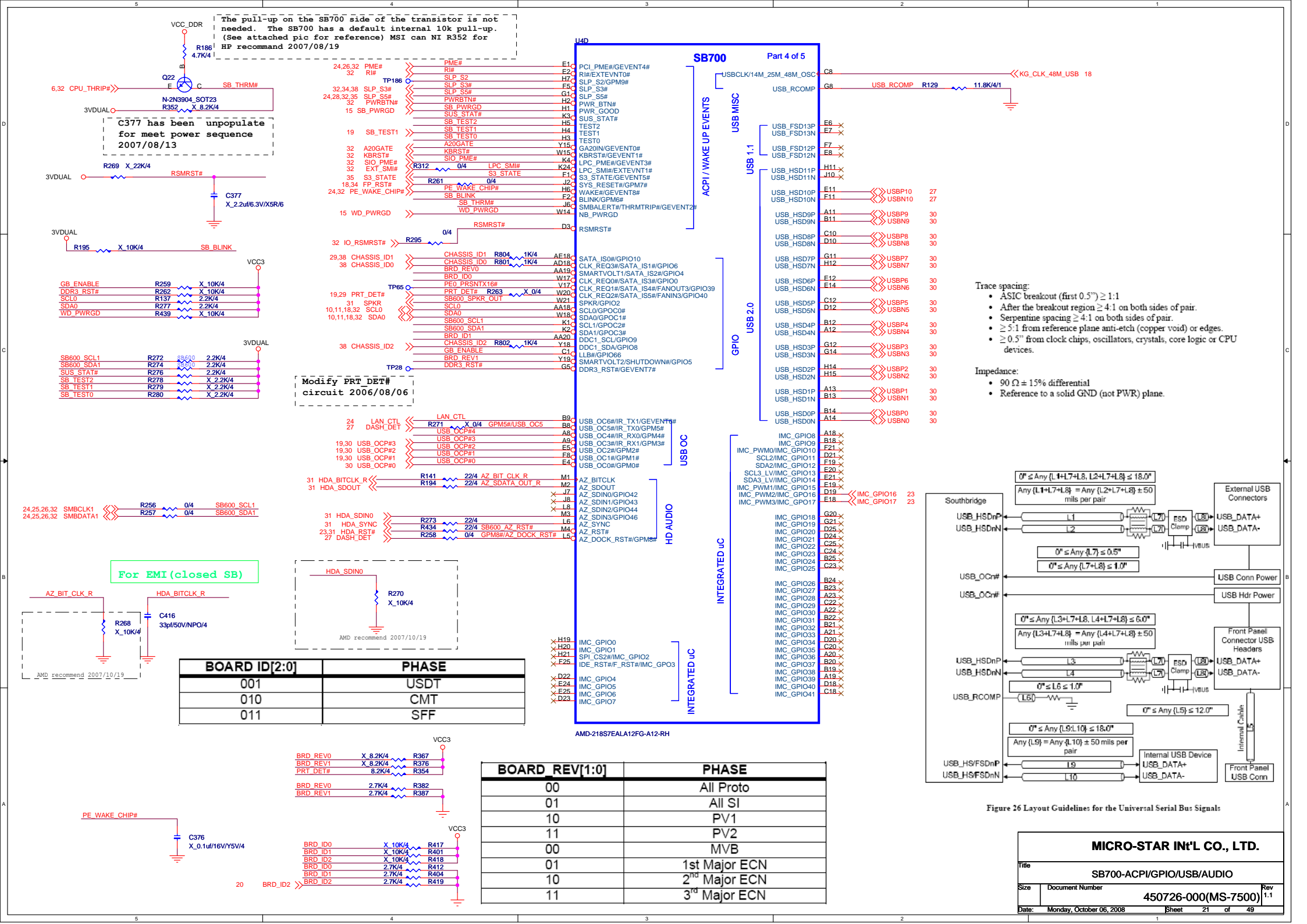
PCI CLKRUN# R247 10K/4
VCC3
Add R140 foe HP
recommnd 2007/10/29



SW50		SLIDE SWITCH OPERATION	
1-3		NORMAL OPERATION	
2-3		CLEAR CMOS	

Added R248 for 3VDUAL
short when clean CMOS
2007/08/06

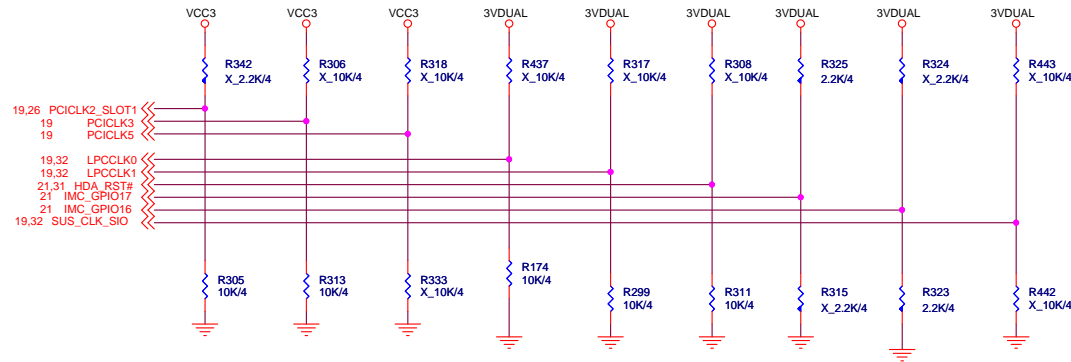






REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK2	PCI_CLK3	PCI_CLK5	LPC_CLK0	LPC_CLK1	AZ_RST#	IMC_GPIO17	IMC_GPIO16
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	RESERVED	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT		L, H = LPC ROM L, L = FWH ROM	

R325 and R323 have been changed from 10K ohm to 2.2K ohm 2007/08/01 (AMD demo schematic update)

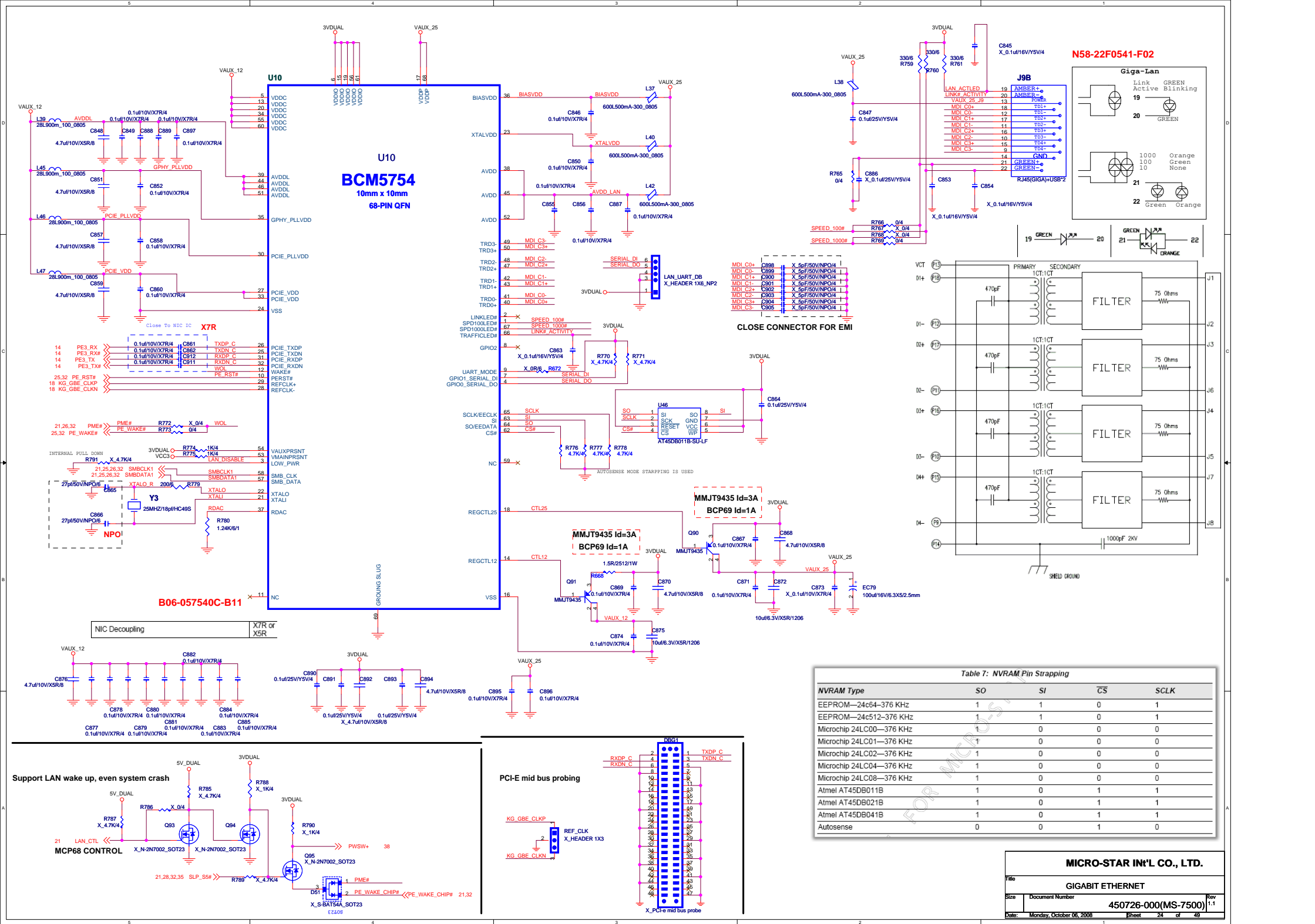
DEBUG STRAPS

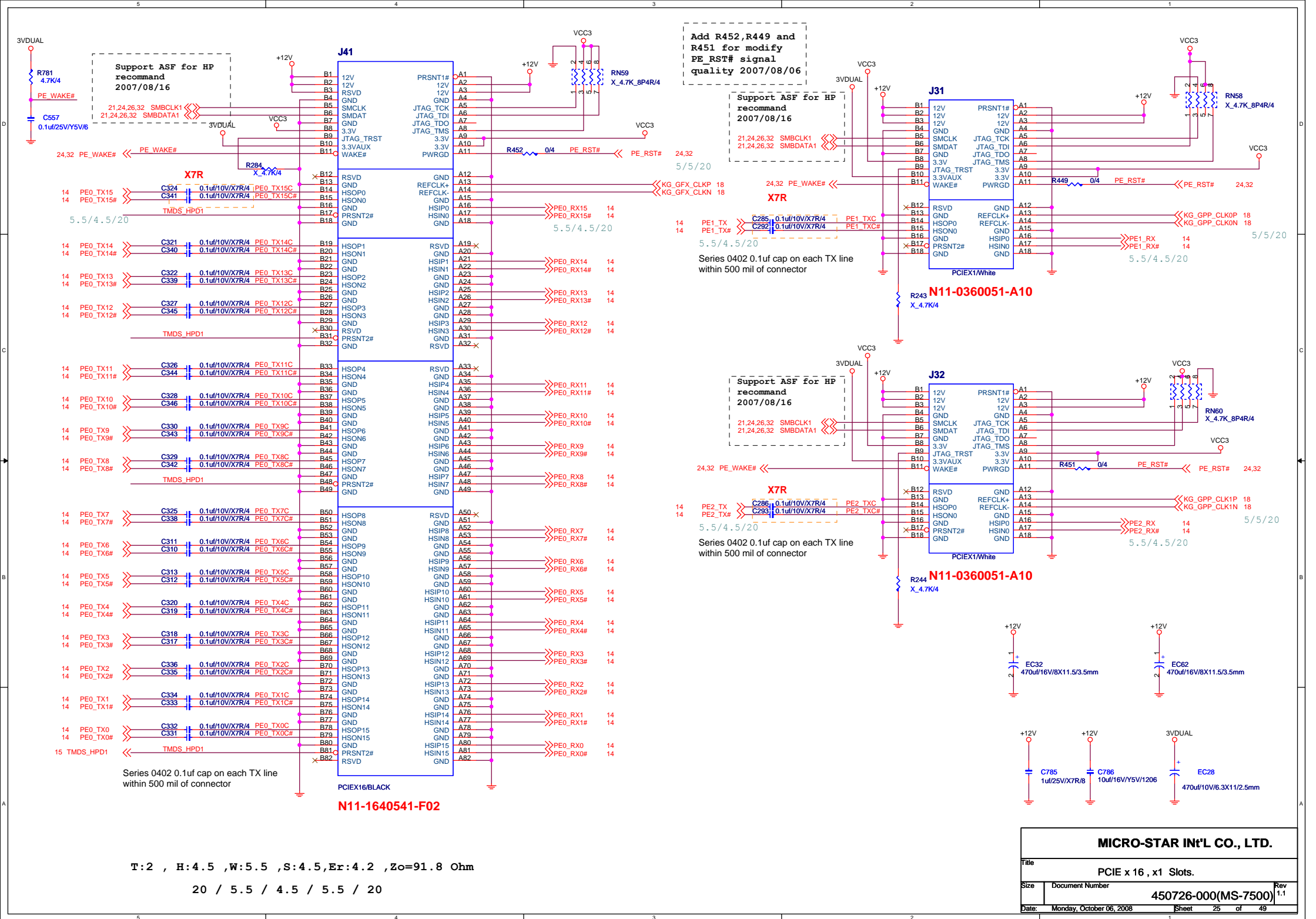
SB700 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

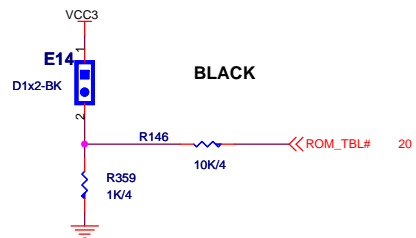
MICRO-STAR INT'L CO., LTD.

File				SB700-STRAPS	
Size	Document Number			450726-000(MS-7500)	Rev 1.1
Date:	Monday, October 06, 2008			Sheet 23	of 49

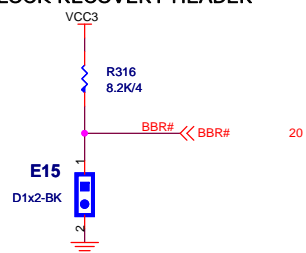




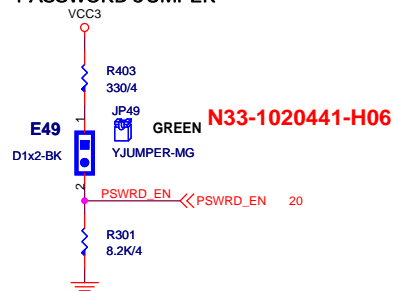
BOOT BLOCK WRITE JUMPER



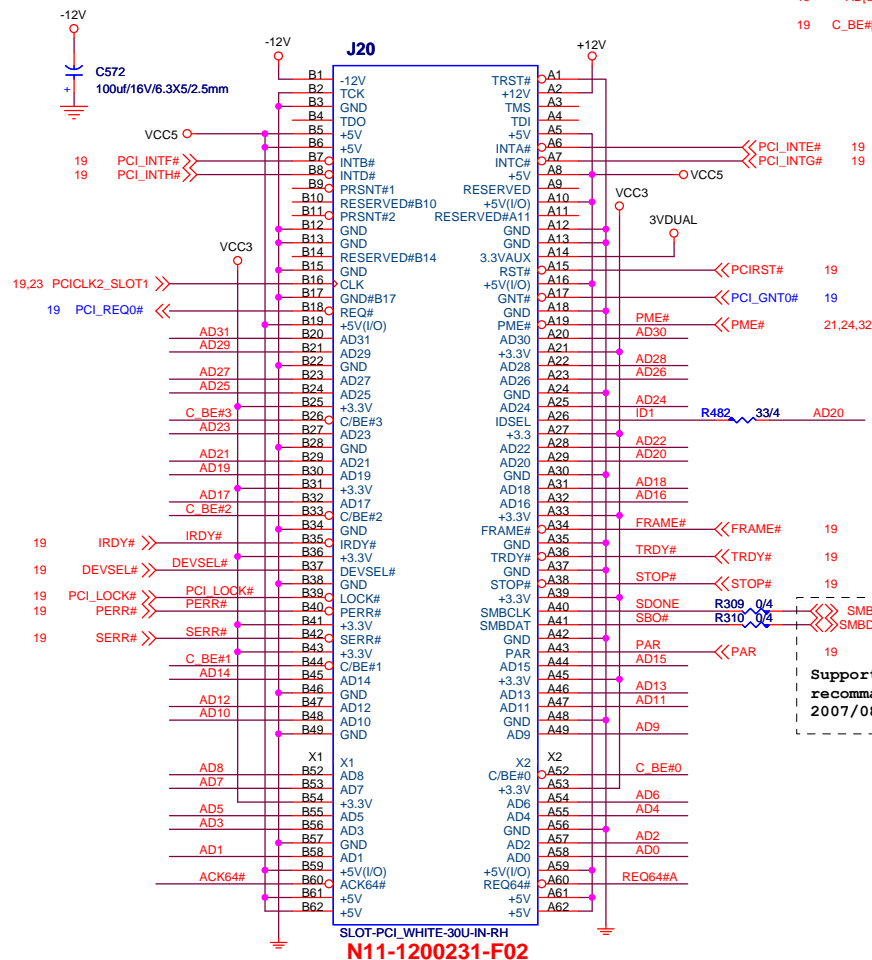
BOOT BLOCK RECOVERY HEADER



PASSWORD JUMPER



PCI SLOT 1 (PCI VER: 2.3 COMPLY)

**SB700**

PCI SLOT1

IDSEL = AD20

PCI REQ0#

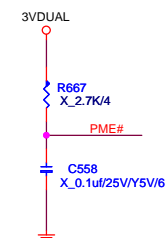
PCI GNT0#

PCI INTE#

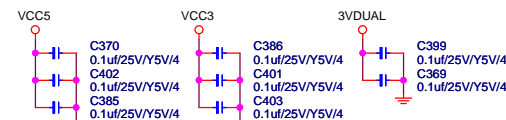
PCIRST#

PCICLK2_SLOT1

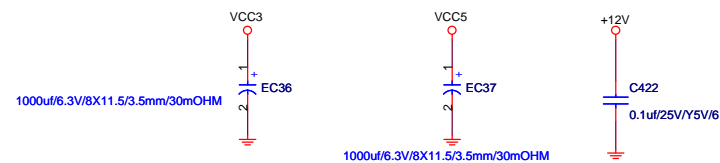
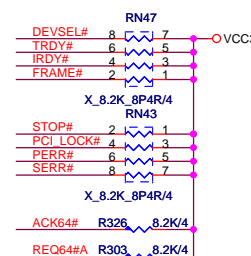
19 AD[31..0] <<>> AD[31..0]
19 C_BE#[3..0] <<>> C_BE#[3..0]



PCI SLOT DECOUPLING CAPACITORS



PCI PULL-UP / DOWN RESISTORS



MICRO-STAR INT'L CO., LTD.

Title			
PCI Slot1			
Size	Document Number	450726-000(MS-7500)	Rev 1.1
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The diagram illustrates the signal traces for the RS780 connector, showing termination and protection components for each signal line. The traces are organized into two main sections: the top section for color signals (RED, GREEN, BLUE) and the bottom section for composite signals (Y, C, COMP).

Top Section (Color Signals):

- RED / RED#:** The signal line is terminated with a resistor to ground. A π filter is shown, consisting of two capacitors to ground and a series resistor. A 3V diode is connected to the signal line after the filter.
- GREEN / GREEN#:** Similar to the red signal, with a termination resistor, a π filter, and a 3V diode.
- BLUE / BLUE#:** Similar to the red and green signals, with a termination resistor, a π filter, and a 3V diode.

Bottom Section (Composite Signals):

- Y:** The signal line is terminated with a resistor to ground. A π filter is shown, consisting of two capacitors to ground and a series resistor. A 3V diode is connected to the signal line after the filter.
- C:** Similar to the Y signal, with a termination resistor, a π filter, and a 3V diode.
- COMP:** Similar to the Y and C signals, with a termination resistor, a π filter, and a 3V diode.

Annotations:

- Place close to VGA/TV connector:** Indicated by an arrow pointing to the top of the diagram.
- Place close to TV connector:** Indicated by an arrow pointing to the bottom of the diagram.
- VGA/TV Connector:** A yellow box on the right side of the top section.
- TV Connector:** A yellow box on the right side of the bottom section.

[illegible][illegible]

Title			
VGA CONNECTOR			
Size	Document Number	450726-000(MS-7500)	Rev 1.1
Date:	Monday, October 06, 2008	Sheet	27 of 49

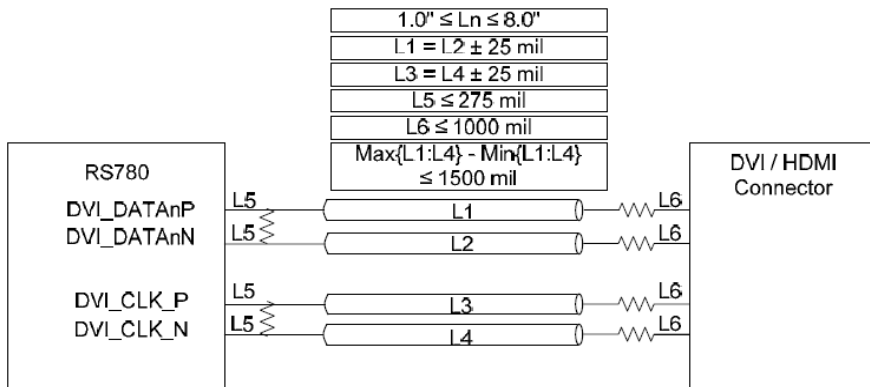
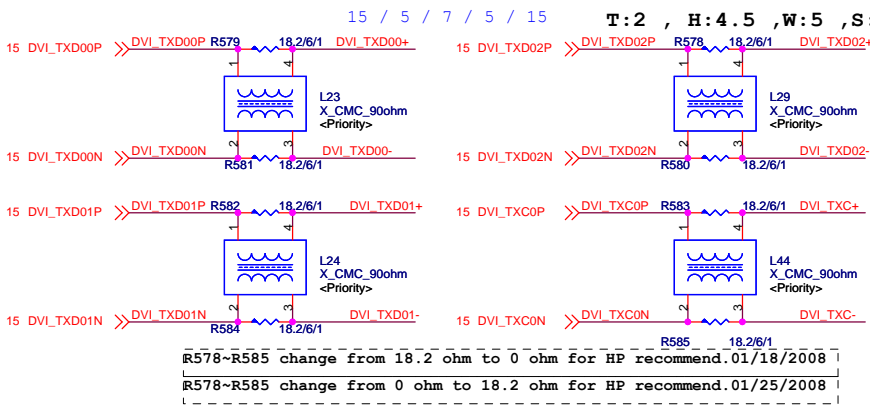
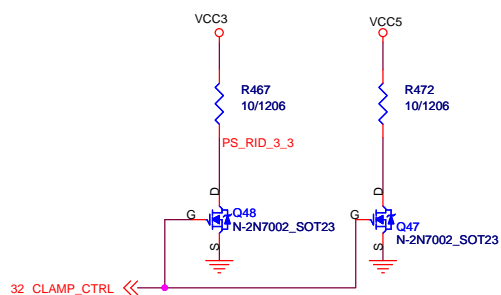


Figure 32: Layout Guidelines for the DVI/HDMI Signals

7.1.6 Residual Voltage Bleed-Off Circuit

A residual voltage circuit is required on the board. This circuit must be active in the S3, S4, and S5 state, whenever the main +5 V and +3.3 V power are turned off. A circuit diagram is shown below. When the system is in S3, S4, or S5, the transistors will be turned on, which will clamp any residual voltage on +5V and +3.3 V to ground. See the figure below for an example of a bleed-off circuit.

BLEED-OFF CIRCUIT



MEMORY VOLTAGE BLEED-OFF CIRCUIT

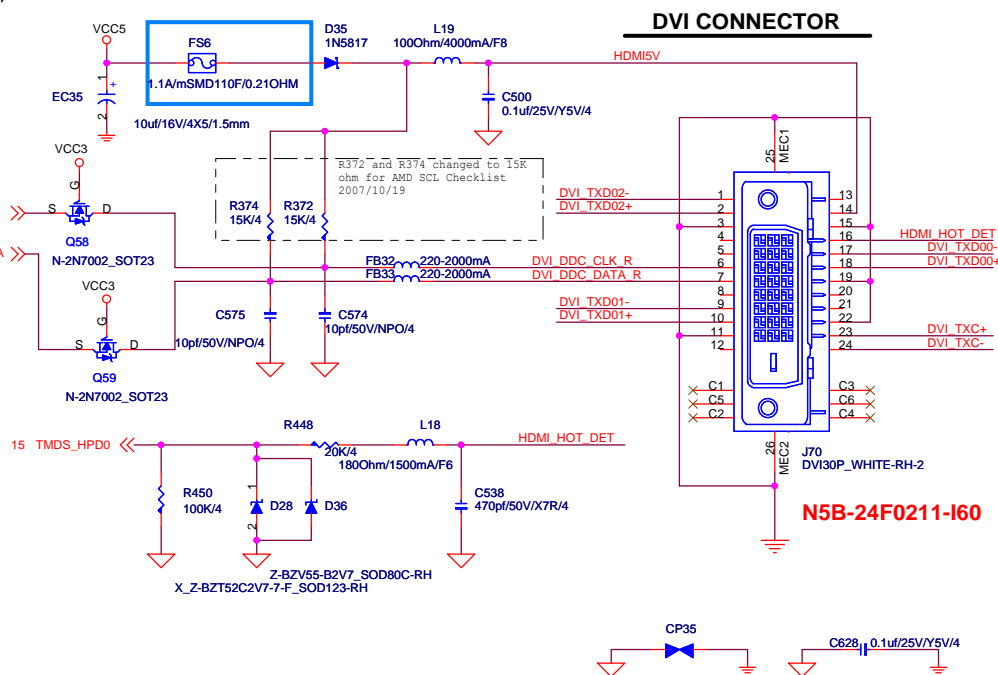
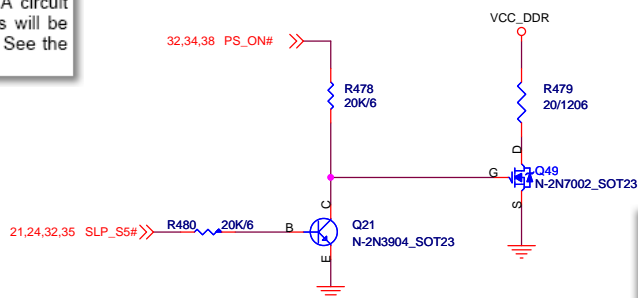


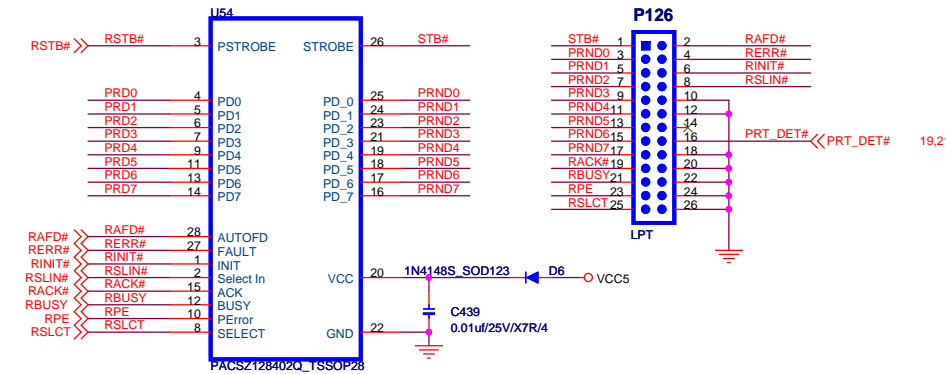
TABLE 38
SYSTEM BOARD LED REQUIREMENTS

Function	Ref Des	Color
+5 V AUX	CR1	Green
+3 V AUX	CR2	Green

MICRO-STAR IN'L CO., LTD.

Title		
DVI CONNECTOR / BLEED OFF		
Size	Document Number	Rev
	450726-000(MS-7500)	1.1
Date:	Monday, October 06, 2008	Sheet 28 of 49

PARALLAL PORT



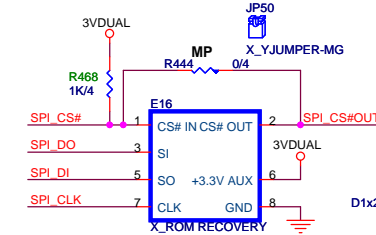
Modify Parallal port circuit 2007/08/13 (Added U54)

TABLE 22
ROM RECOVERY HEADER DEFINITION

E16			
PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	CS# IN	CS# OUT	2
3	SI	KEY (no pin)	4
5	SO	VCC (+3.3V AUX)	6
7	CLK	GND	8

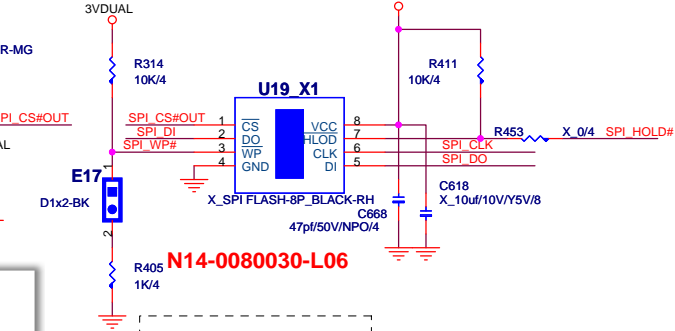
SPI ROM

20 SPI_DI
20 SPI_DO
20 SPI_CLK
20 SPI_CS#
20 SPI_HOLD#



Modify SPI HOLD# circuit for
AMD recommend 2007/08/01

Connect E16 pin1 and pin2



Added E17 2007/08/13

N14-0080030-L06

J17
JUMPER-1X2A_BLACK-RH

BIOS

U19
SPI/8M/SOP8

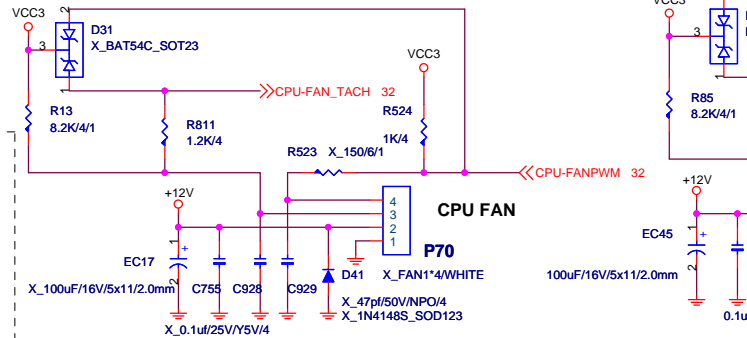
Parallel Port 2 x13 header

PIN #	SIGNAL NAME	SIGNAL NAME	PIN #
1	LPT_STB#	XAFD#	2
3	LPT_SPD0	ERROR#	4
5	LPT_SPD1	XINIT#	6
7	LPT_SPD2	XSLIN#	8
9	LPT_SPD3	GND	10
11	LPT_SPD4	GND	12
13	LPT_SPD5	GND	14
15	LPT_SPD6	PRT_DET#	16
17	LPT_SPD7	GND	18
19	ACK#	GND	20
21	BUSY	GND	22
23	PE	LDT_RST#	24
	SLCT	GND	26

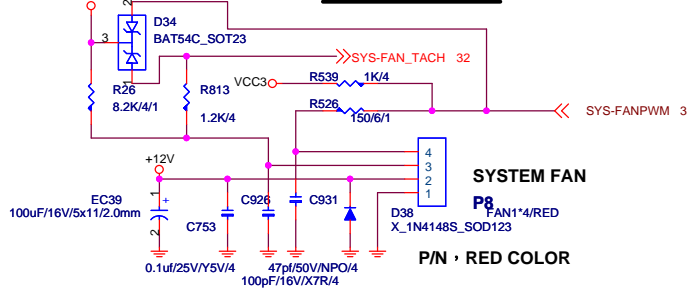
FAN BOLCK

Modify Fan-circuit for HP recommend 2007/08/06

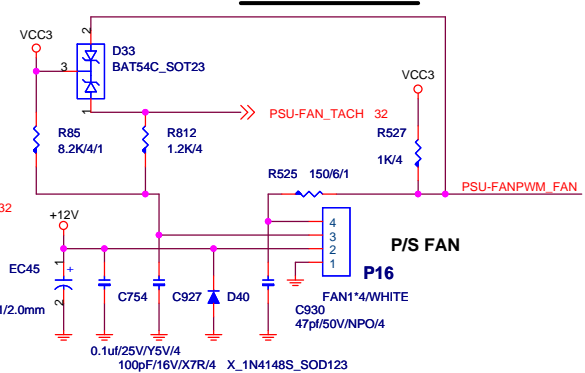
CPU FAN



SYS FAN



PSU FAN



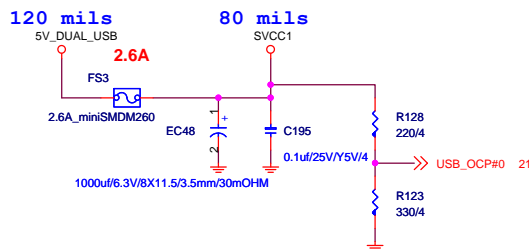
Pin #	Signal Name
1	GND
2	+12V
3	FAN TACH
4	FAN PWM INPUT

MICRO-STAR IN'L CO., LTD.

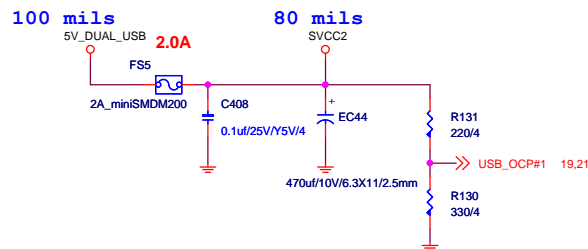
Title			SPI ROM / FAN / LPT
Size	Document Number	450726-000(MS-7500)	
Date:	Monday, October 06, 2008	Sheet	29 of 49

Modify FAN-PWM duty cycle inverter circuit for HP recommend 2007/08/13

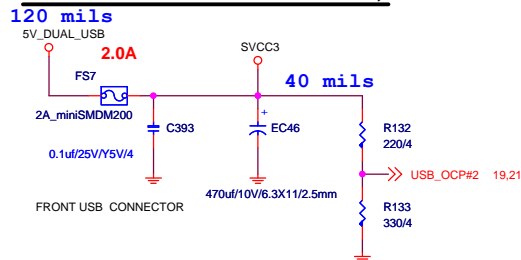
POWER CIRCUIT FOR USB PORT 0,1,2,3



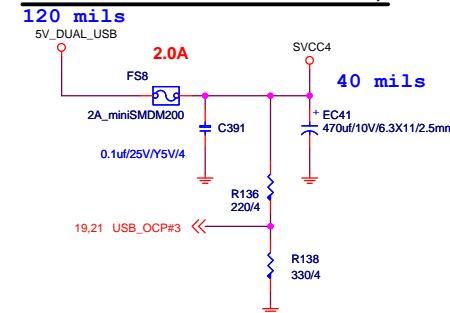
POWER CIRCUIT FOR USB PORT 4,5



POWER CIRCUIT FOR USB PORT 6,7

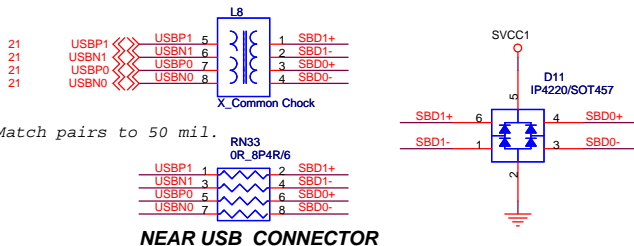


POWER CIRCUIT FOR USB PORT 8,9



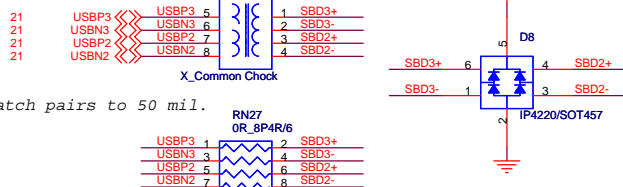
REAR PANEL USB CONNECTOR FOR USB PORT 0,1,2,3

Trace lengths must be less 12 inches



NEAR USB CONNECTOR

Trace lengths must be less 12 inches

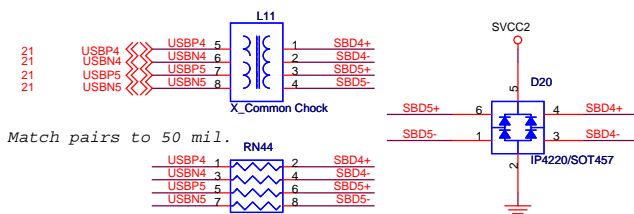


NEAR USB CONNECTOR

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

REAL USB CONNECTOR WITH RJ45 FOR USB PORT 4,5

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

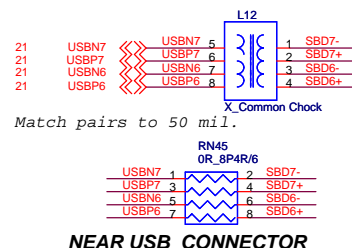
T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm
20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

FRONT PANEL USB CONNECTOR FOR USB PORT 6,7

Trace lengths must be less 5 inches



NEAR USB CONNECTOR

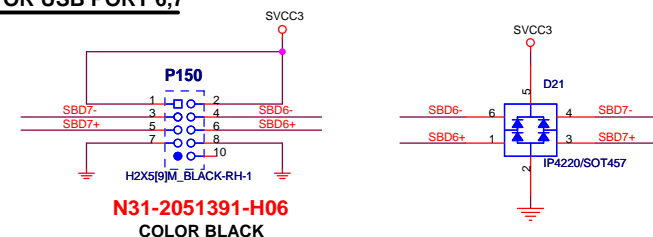
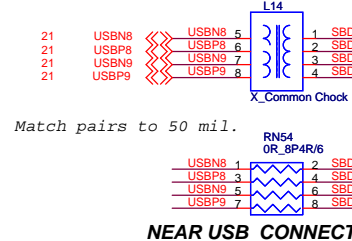


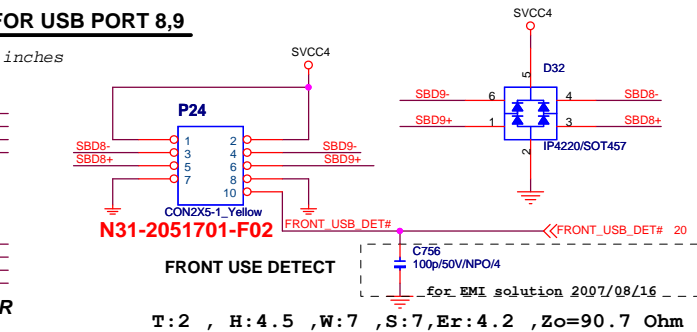
TABLE 10 MEDIA CARD READER USB HEADER DEFINITION (TOP VIEW)			
P150			
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 4 (-)	USB Port 5 (-)	4
5	USB Port 4 (+)	USB Port 5 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	No Connect	10

FRONT PANEL USB CONNECTOR FOR USB PORT 8,9

Trace lengths must be less 5 inches



NEAR USB CONNECTOR



T:2 , H:4.5 ,W:7 ,S:7,Er:4.2 ,Zo=90.7 Ohm

20 / 7 / 7 / 7 / 20 / 7 / 7 / 7 / 20

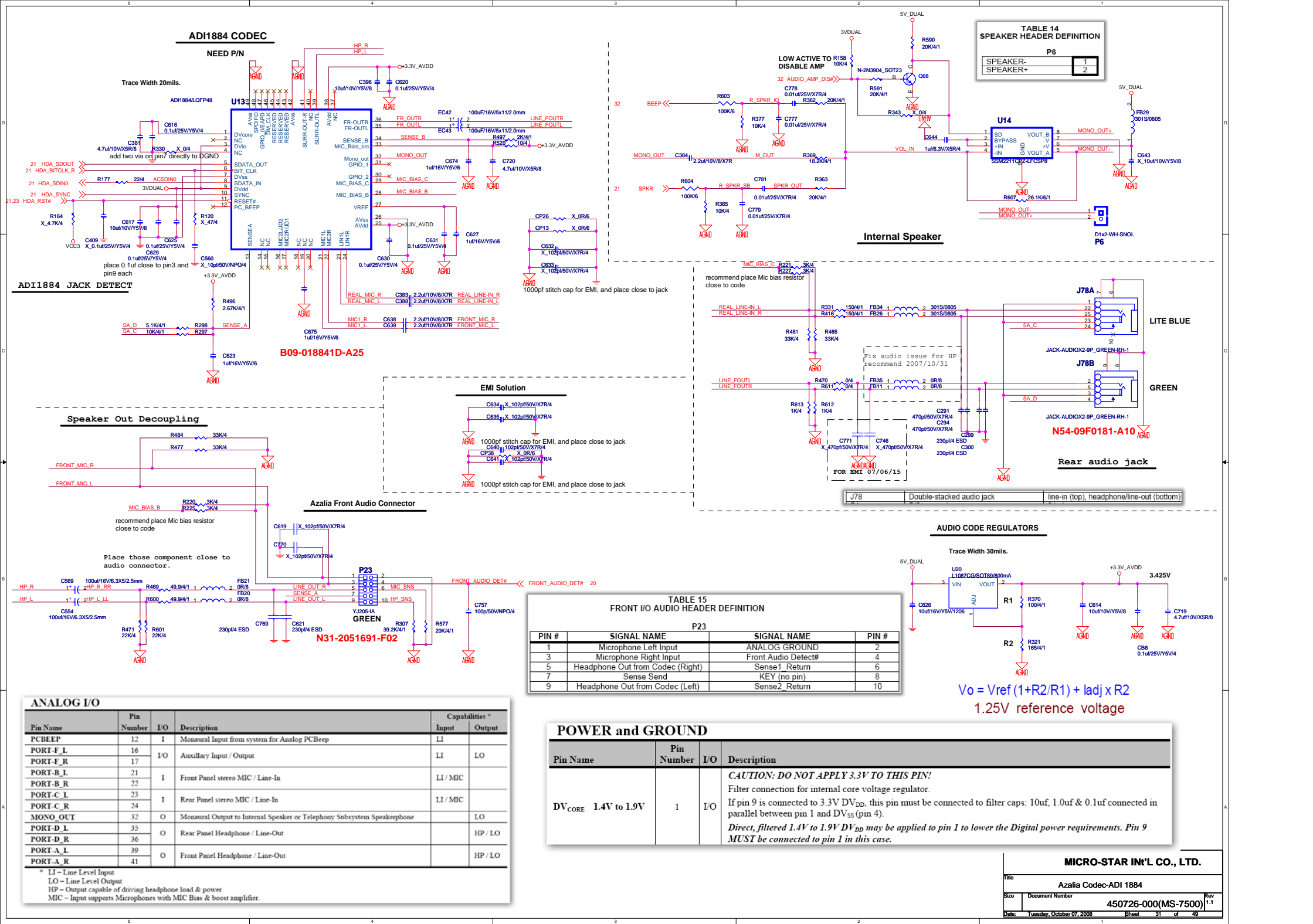
TABLE 9 FRONT I/O USB HEADER DEFINITION (TOP VIEW)			
P24			
Pin #	Signal Name	Signal Name	Pin #
1	+5 V (Fused)	+5 V (Fused)	2
3	USB Port 8 (-)	USB Port 9 (-)	4
5	USB Port 8 (+)	USB Port 9 (+)	6
7	GROUND	GROUND	8
9	KEY (no pin)	FRONT USB DETECT#	10

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USB Conn.

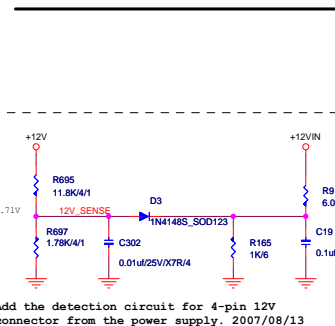
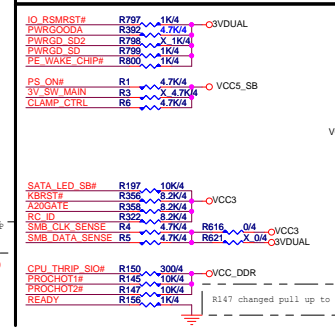
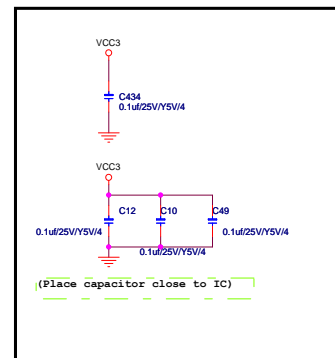
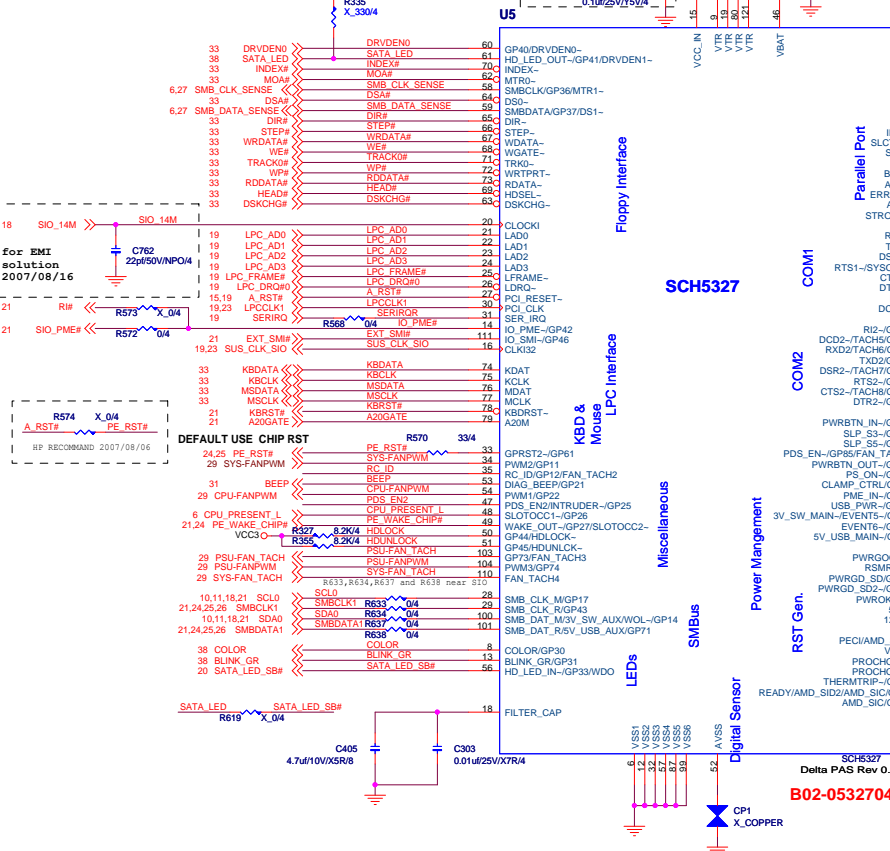
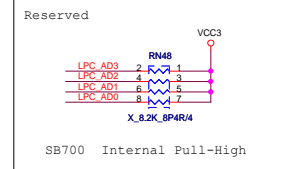
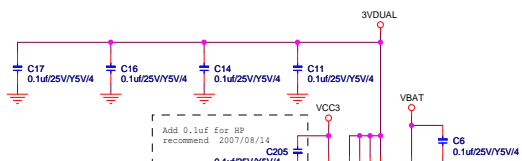
Size Document Number 450726-000(MS-7500) Rev 1.1

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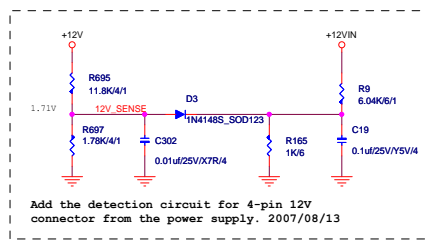
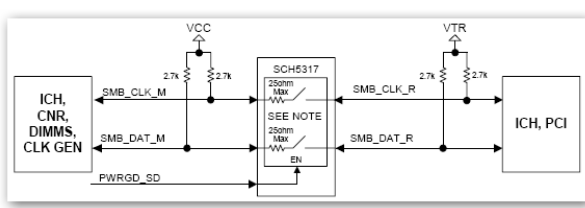
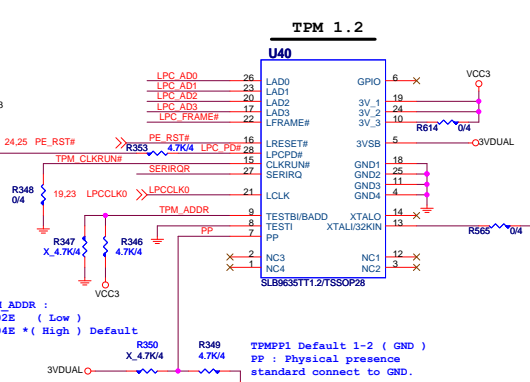


LPC length should be less than 18 inches.

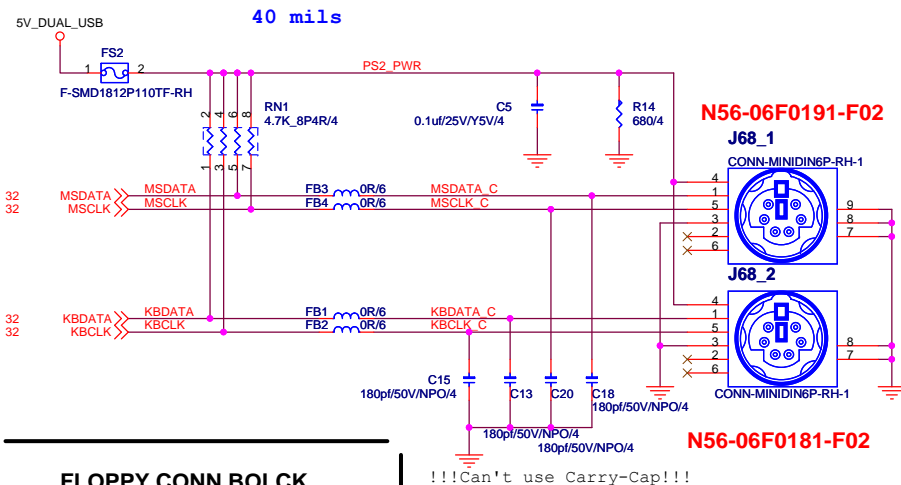
LPC SUPER I/O SMSC 5327



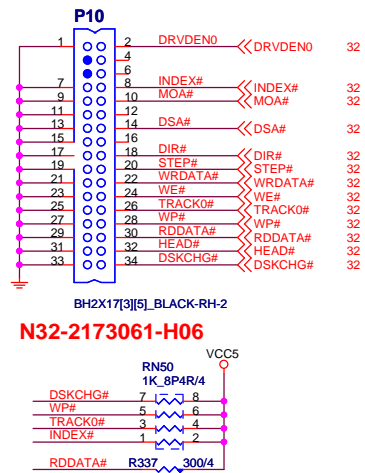
3V3DUAL R2 4.7K4 PWRBTN# SB700 Internal Pull-High
installed R2 for AMD recommend 2007/10/19



PS2 KEYBOARD & MOUSE CONNECTOR

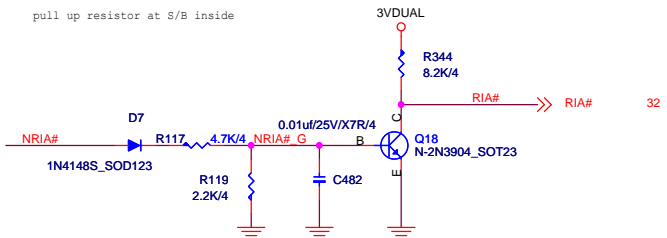


FLOPPY CONN BOLCK



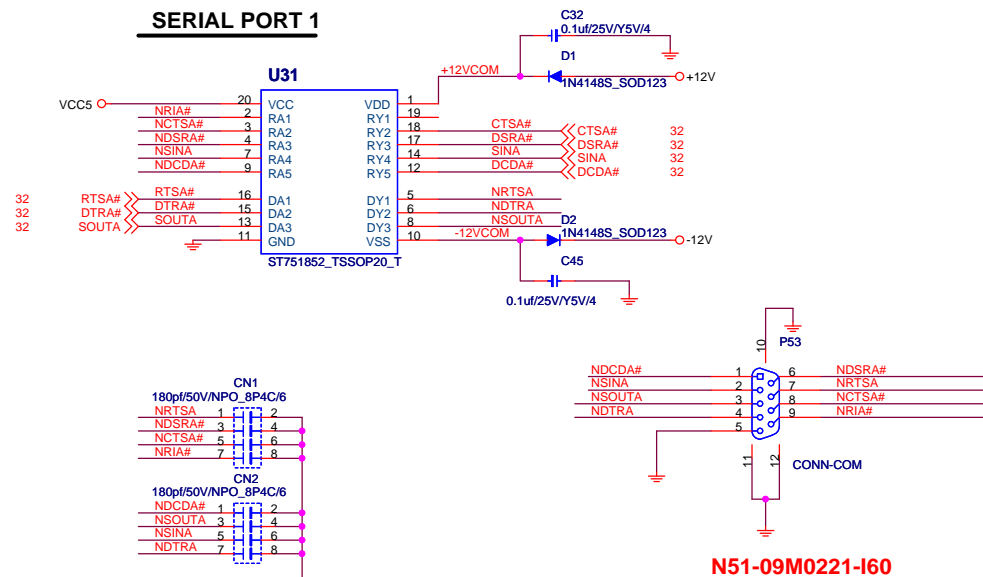
Support ring wake up

pull up resistor at S/B inside



Modify Ring circuit for HP recommend 2007/08/13

SERIAL PORT 1



SERIAL PORT 2

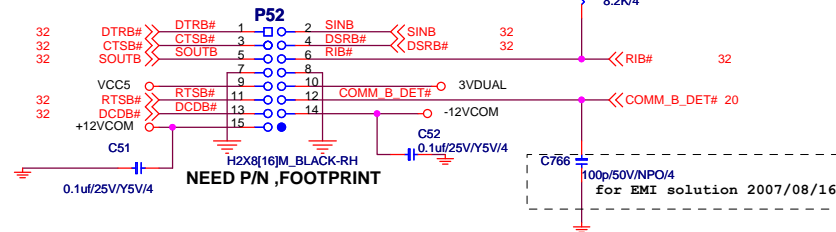
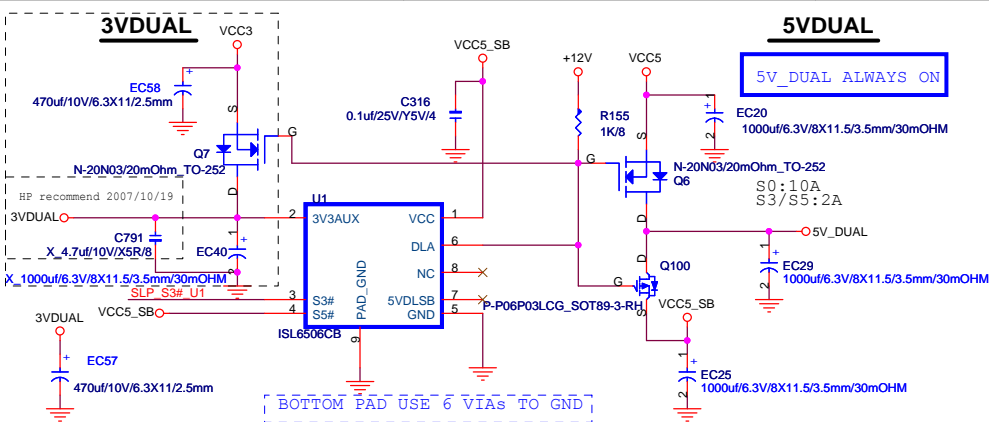


TABLE 12
FLOATING SERIAL PORT PIN DEFINITION (TOP VIEW)

P52			
Pin #	Signal Name	Signal Name	Pin #
1	DTR#	RXD	2
3	CTS#	DSR#	4
5	TXD	RI#	6
7	GND	GND	8
9	+5 V	+3.3 VAUX	10
11	RTS#	COMM B DETECT#	12
13	DCD#	-12 V (THRU DIODE)	14
15	+12 V (THRU DIODE)	KEY	16

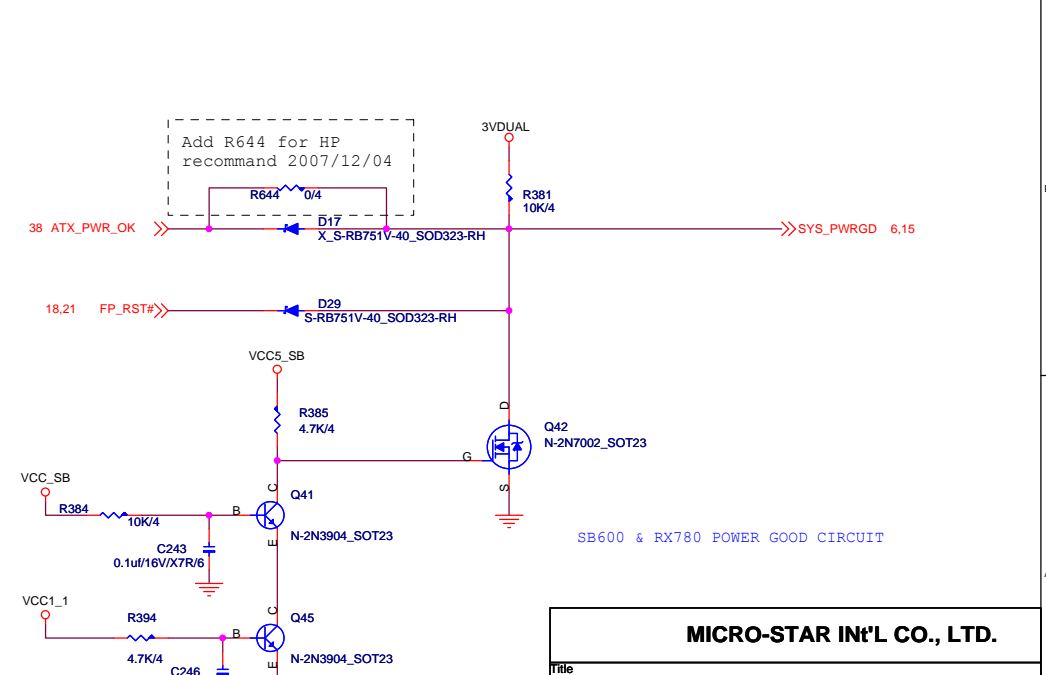
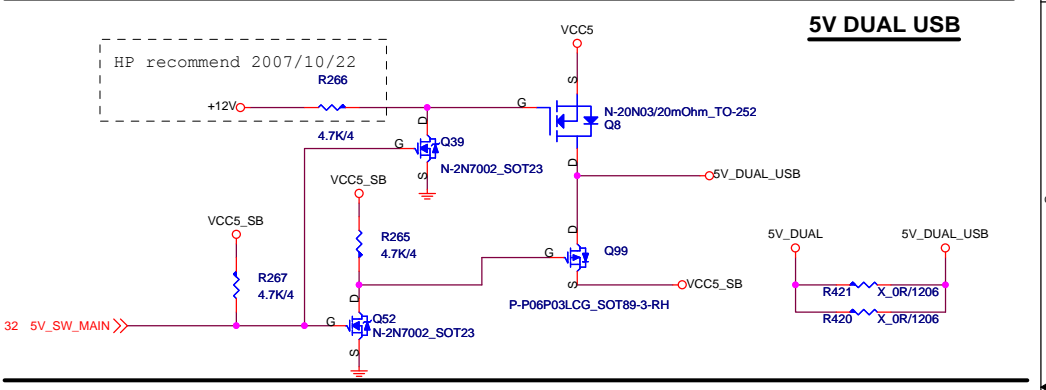
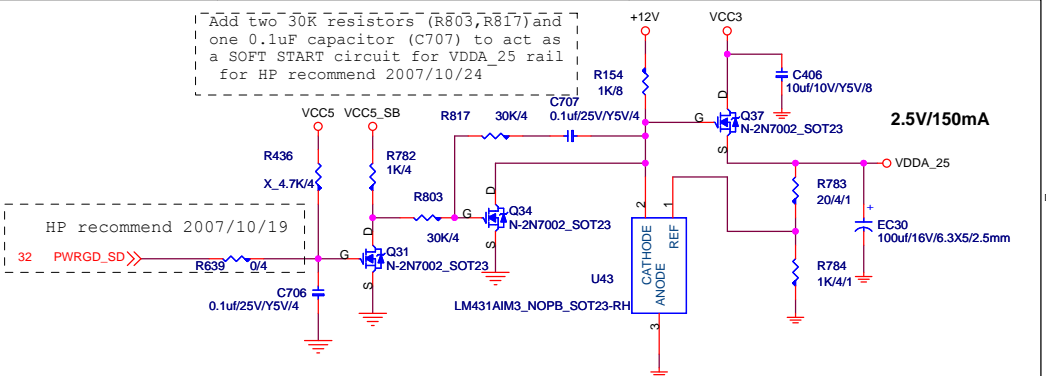
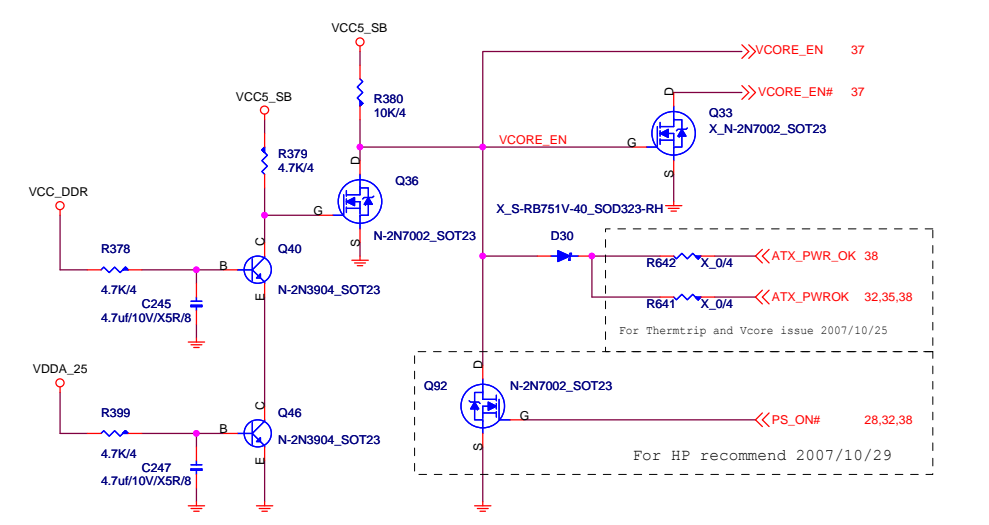
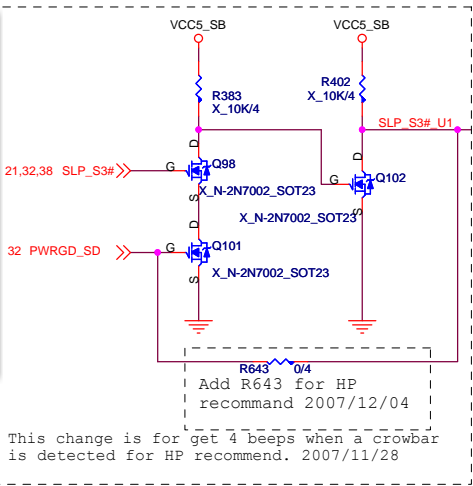
MICRO-STAR IN'L CO., LTD.

Title			
KB/MS&COM1&Floppy Conn.			
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ACPI POWER STATE SUPPORT

Voltage	S0/S1	S3	S4/S5	S5	No AC
3.3 V Main	On	Off	Off	Off	Off
5 V Main	On	Off	Off	Off	Off
12 V	On	Off	Off	Off	Off
-12 V	On	Off	Off	Off	Off
CPU Core Voltage	On	Off	Off	Off	Off
RS780 core/SB800	On	Off	Off	Off	Off
1.8 V DDR2_VDDQ	On	On	On	Off	Off
0.9 V DDR2_VTT	On	On	On	On	Off
5 V Standby	On	On	On	On	Off
3.3 V Standby	On	On	On	On	Off
5 V Dual (USB-PS/2)	On - main	On - aux	On	Off	Off
5 V Dual (Memory)	On - main	On - aux	On - aux	Off	Off
3.3 V Dual (PCI)	On - main	On - aux	On - aux	On - aux	Off
3.3 V LAN (EPW)	On	On	On	On	Off
3.3 V Digital Audio	On	On	Off	Off	Off
5 V Analog Audio	On	Off	Off	Off	Off
Battery/RTC Voltage	On	On	On	On	On



DDR II 1.8V POWER

Irms(MAX) of VCC_DDR=18A

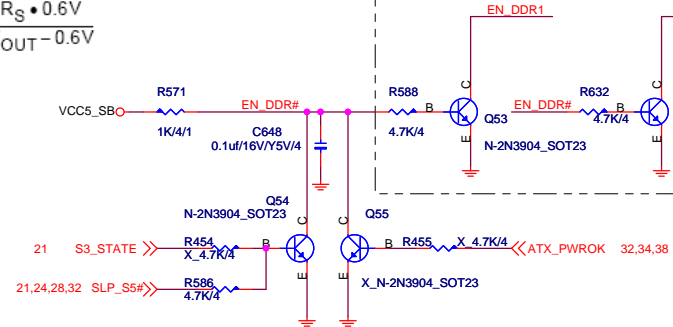
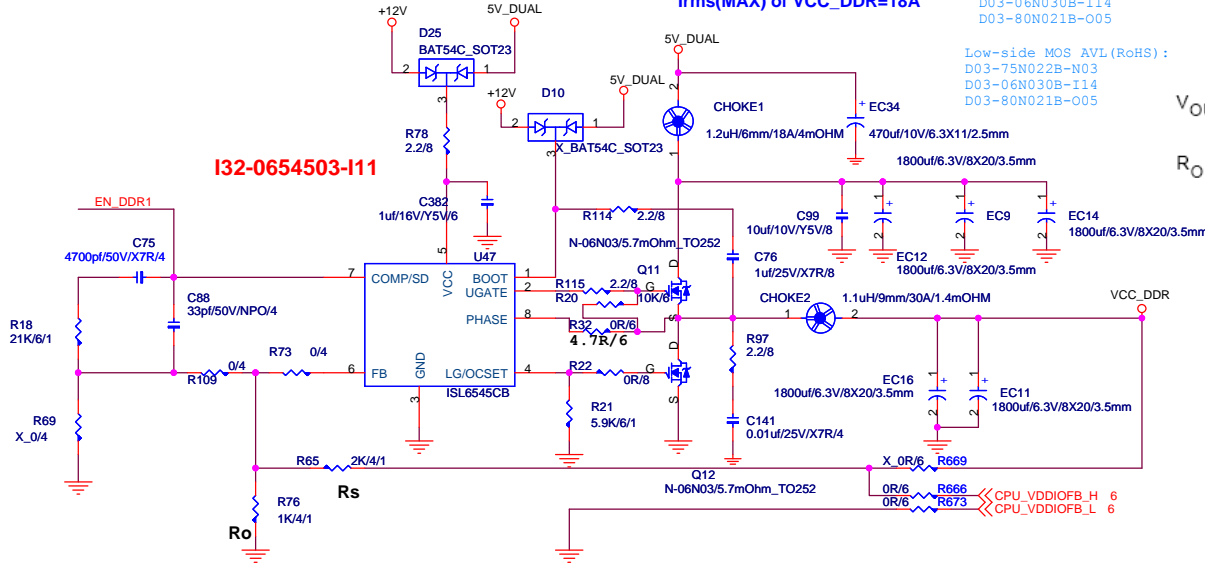
High-side MOS AVL (RoHS) :
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

Low-side MOS AVL (RoHS) :
D03-75N022B-N03
D03-06N030B-I14
D03-80N021B-O05

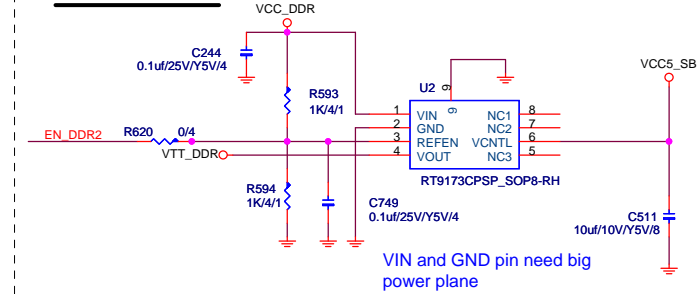
$$V_{OUT} = 0.6V \cdot \frac{(R_S + R_O)}{R_O}$$

$$R_O = \frac{R_S \cdot 0.6V}{V_{OUT} - 0.6V}$$

I32-0654503-I11

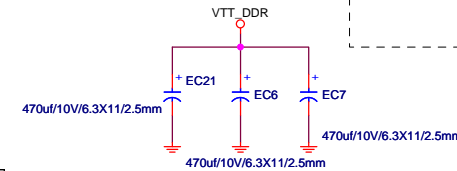


DDR VTT Power



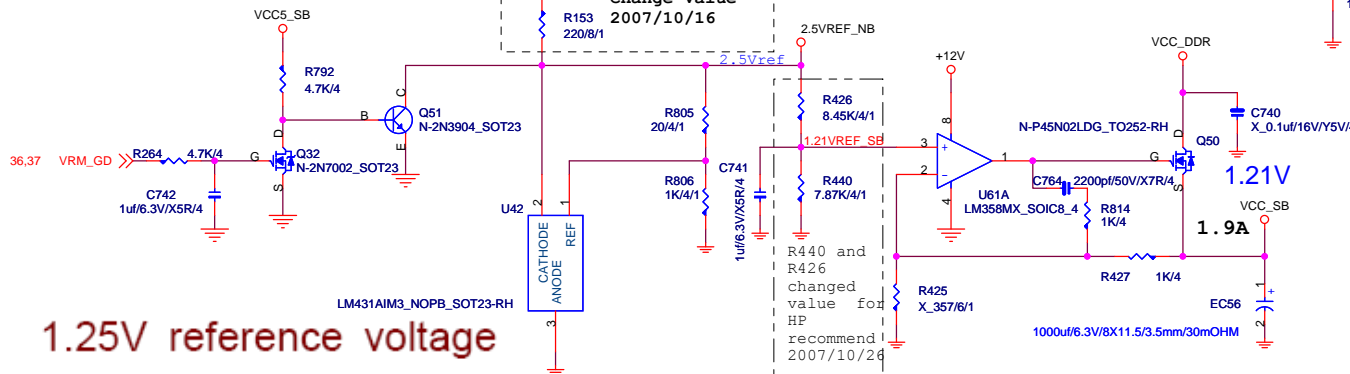
$$I_{PEAK} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{r_{DS(ON)}}$$

where I_{OCSET} is the internal OCSET current source (21.5μA)



SHUTDOWN CONTROL					
Shutdown Pin Enable Threshold	-	VSD	1.14	1.24	1.34
			V		

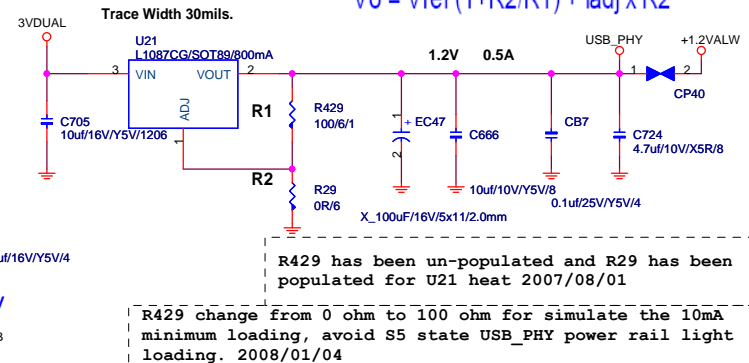
Modify current
too weak
2007/08/01
Change Value
2007/10/16



1.25V reference voltage

I31-0520803-O05

$$V_o = V_{ref} (1 + R2/R1) + I_{adj} \times R2$$



R429 has been un-populated and R29 has been populated for U21 heat 2007/08/01

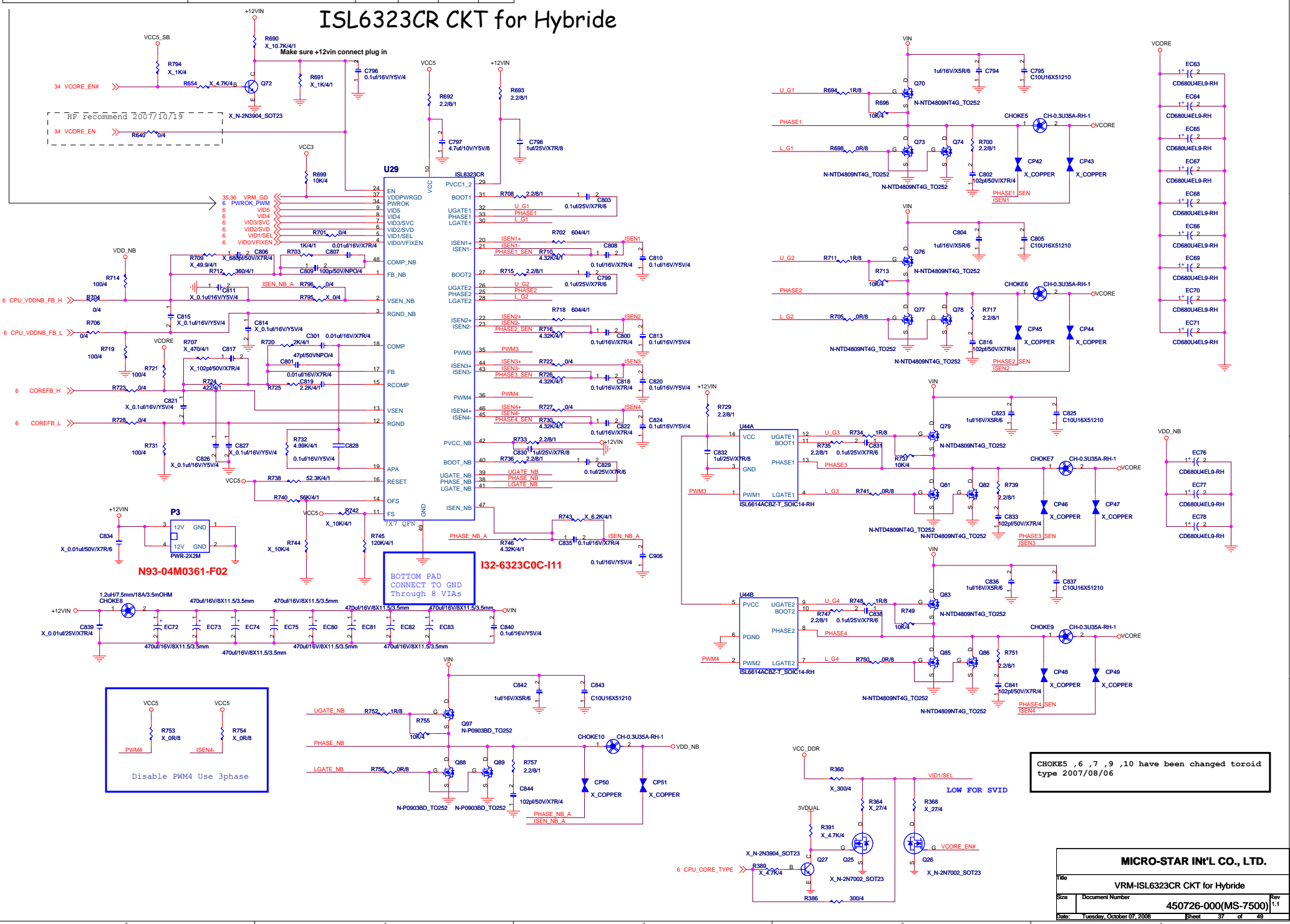
R429 change from 0 ohm to 100 ohm for simulate the 10mA minimum loading, avoid S5 state USB_PHY power rail light loading. 2008/01/04

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Sys. Regulators / DDR			
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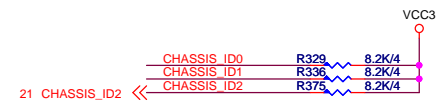
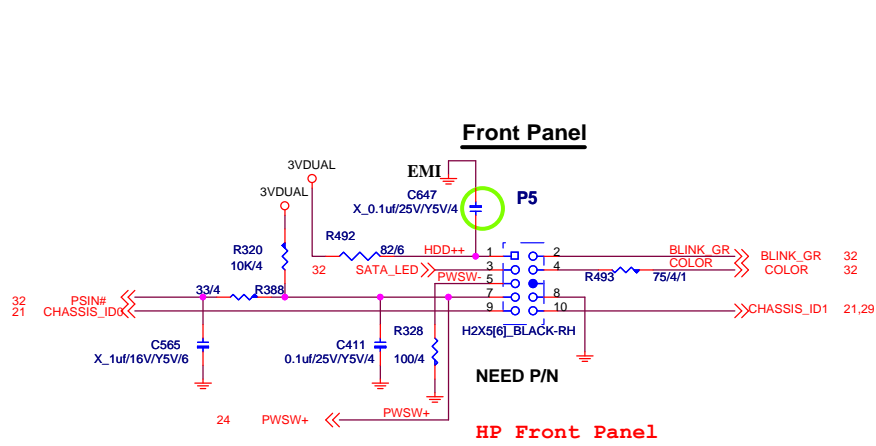
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWROK Input HIGH Threshold		2	-	-	V
PWROK Input LOW Threshold		-	-	0.8	V

ISL6323CR CKT for Hybride



CHOKES ,6 ,7 ,9 ,10 have been changed toroid
type 2007/08/06

MICRO-STAR INT'L CO., LTD.			
Title VRM-ISL6323CR CKT for Hybride			
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HD_LED +	1	2	PWR_LED + (BLINK)
HD_LED -	3	4	PWR_LED - (COLOR)
GND	5	6	(key)
POWER_BUTTON#	7	8	GND
CHASSIS_ID0	9	10	CHASSIS_ID1

ATX Connector

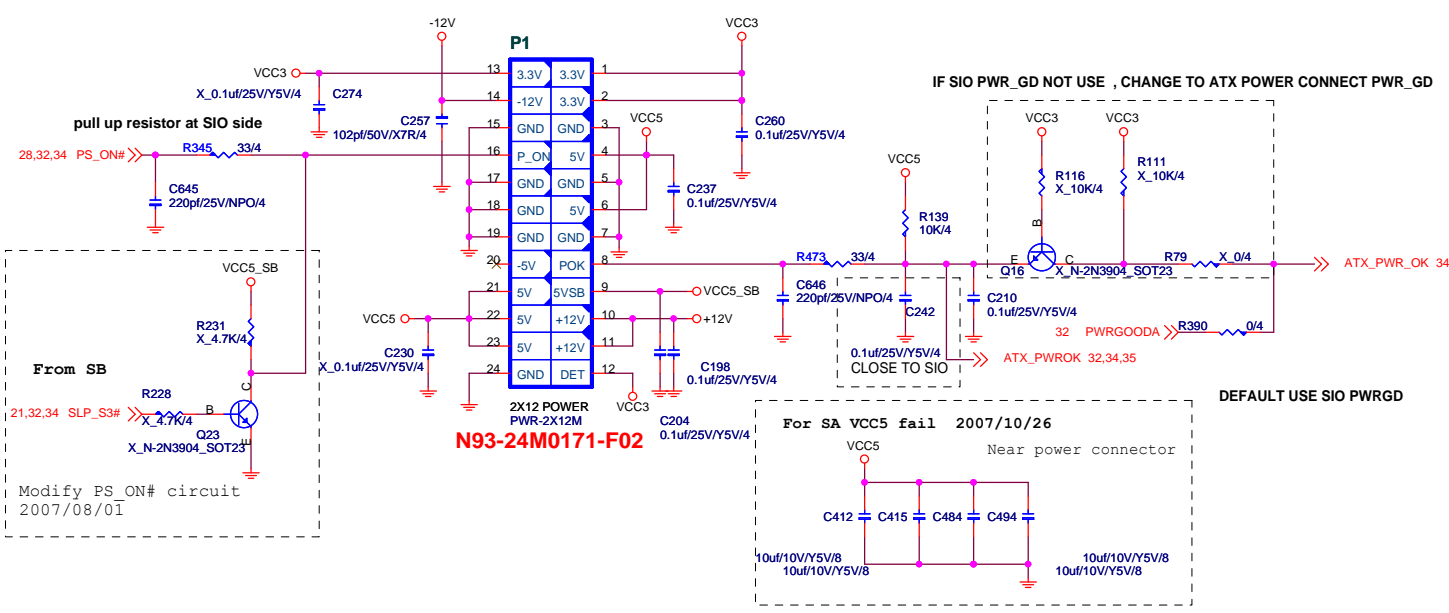
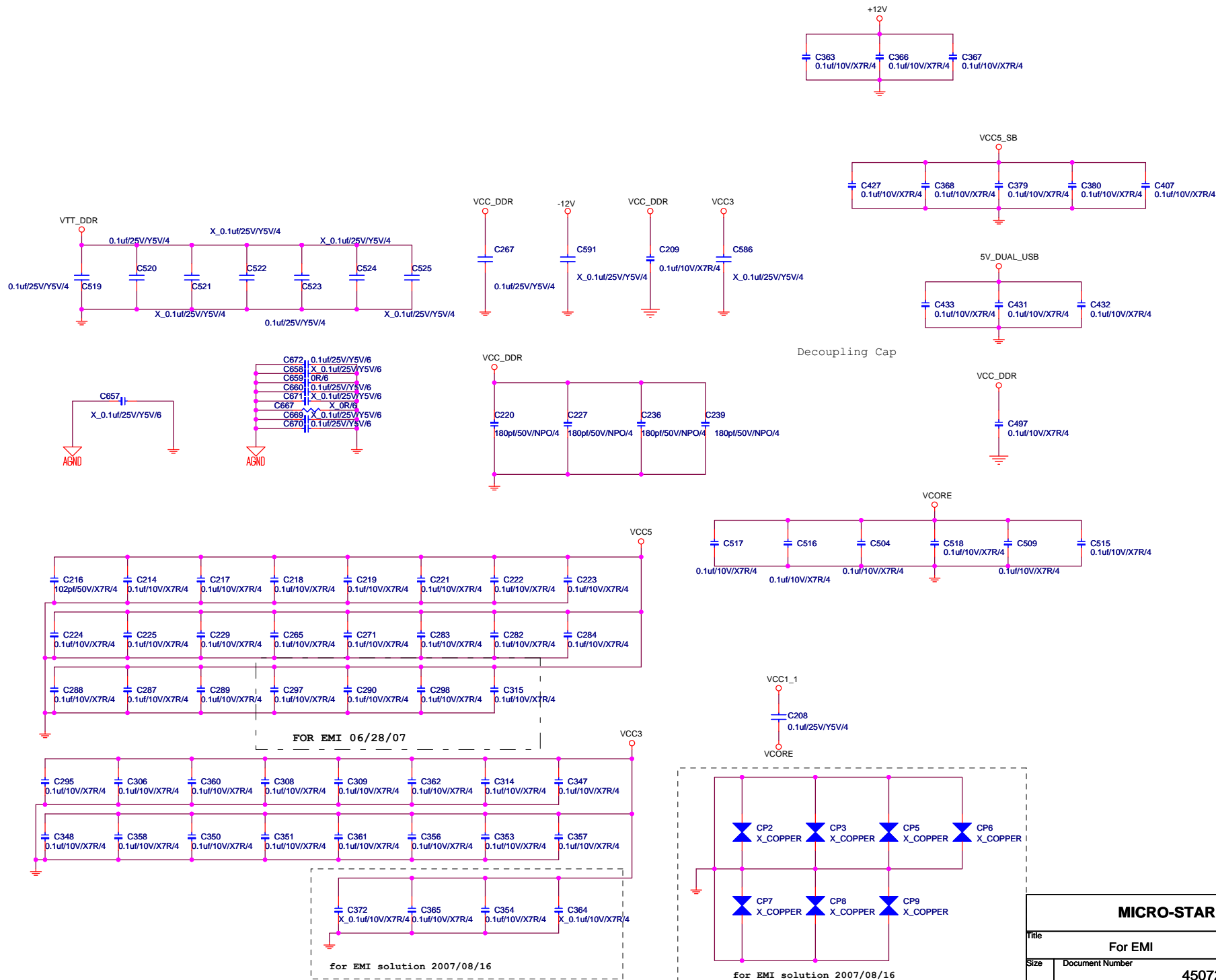


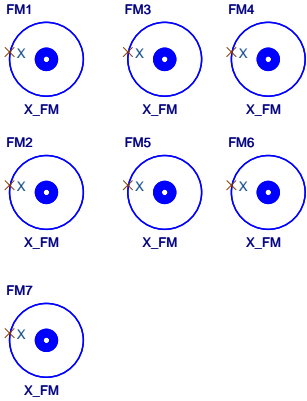
TABLE 5
POWER SUPPLY CONNECTOR PINOUT

	P1		
+3.3 V	13	1	+3.3 V
-12 V	14	2	+3.3 V
GND	15	3	GND
PSON#	16	4	+5 V
GND	17	5	GND
GND	18	6	+5 V
GND	19	7	GND
NOT USED	20	8	POWER OK
+5 V	21	9	+5 V STANDBY
+5 V	22	10	+12 V
+5 V	23	11	+12 V
GND	24	12	+3.3 V

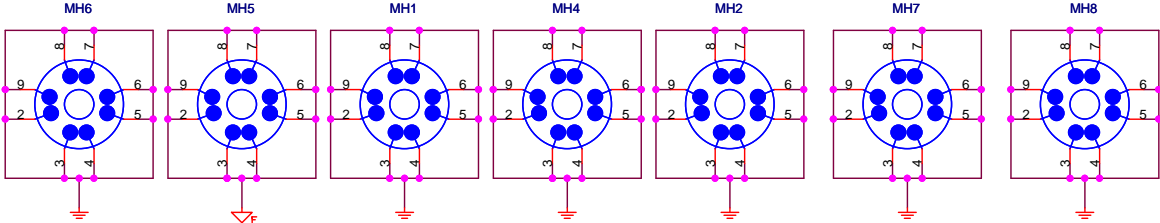


MICRO-STAR IN'L CO., LTD.			
Title For EMI			
Size	Document Number		Rev
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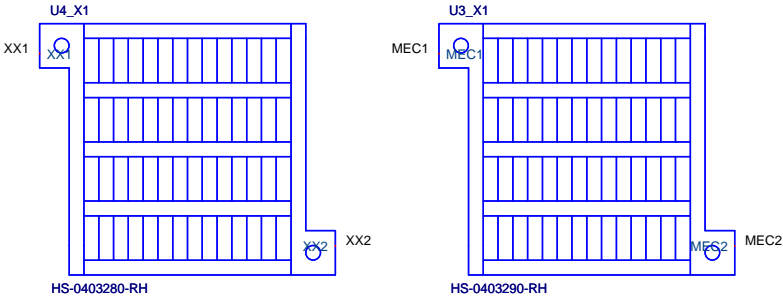
Optics Orientation Holes



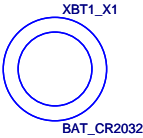
Mounting Holes



NB/SB FAN/HEAT-SINK



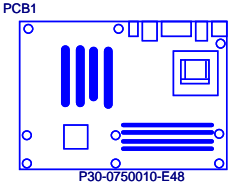
BATTERY



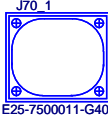
Simulation



PCB

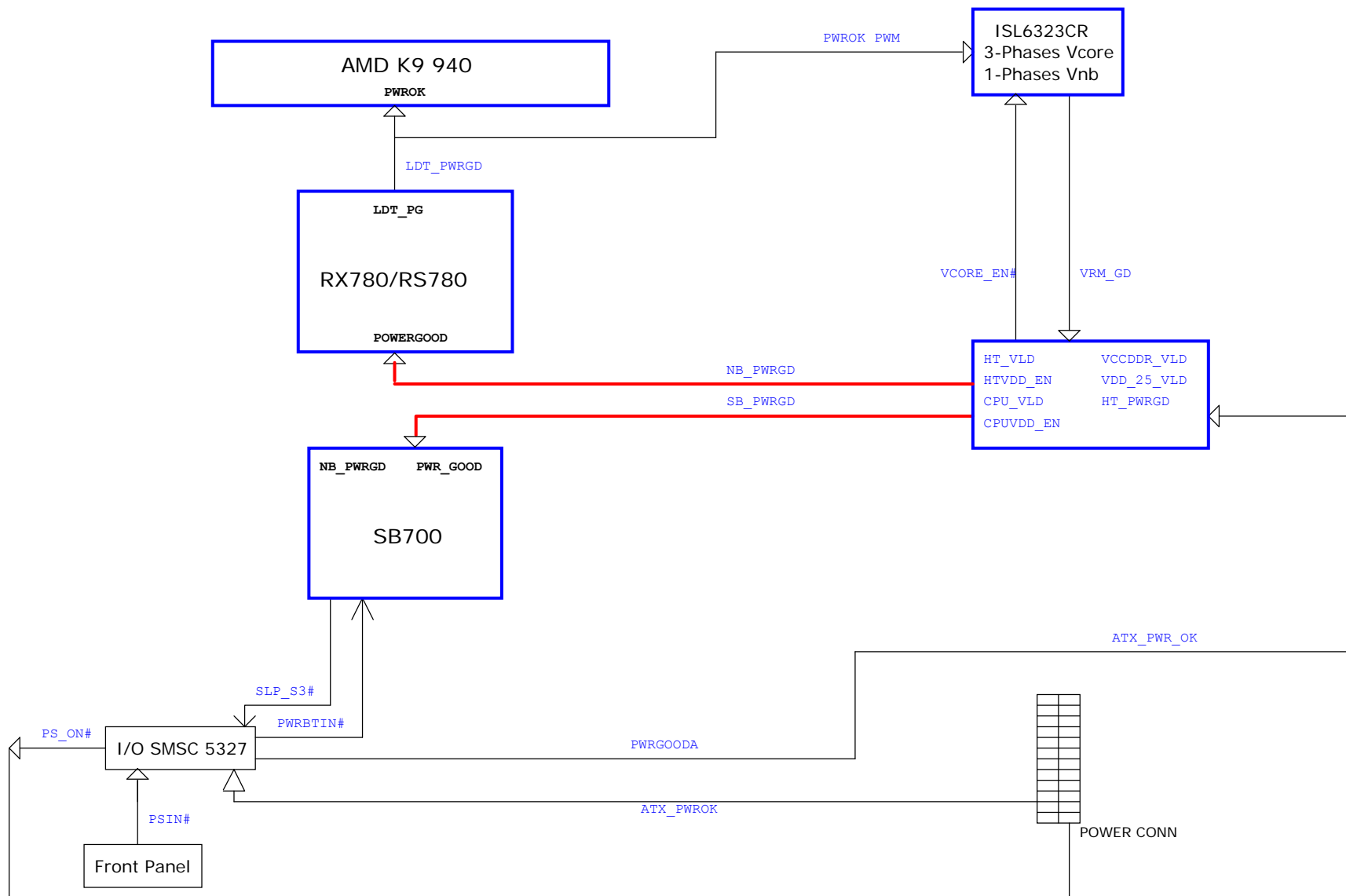


DVI gasket

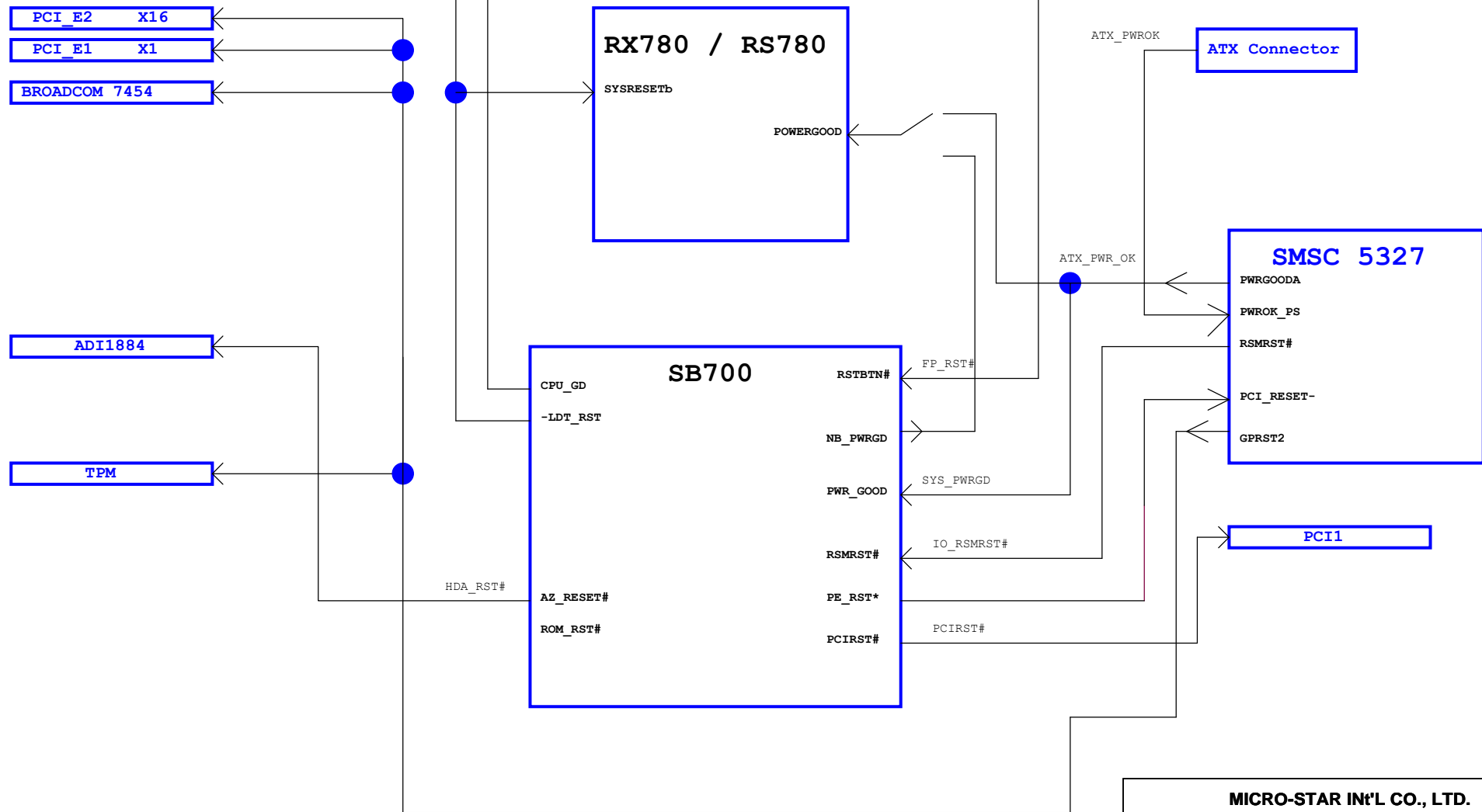


MICRO-STAR INT'L CO., LTD.			
Title			
BOM - Option Parts			
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PWROK MAP



RESET MAP



MICRO-STAR IN'L CO., LTD.

Title			RESET MAP
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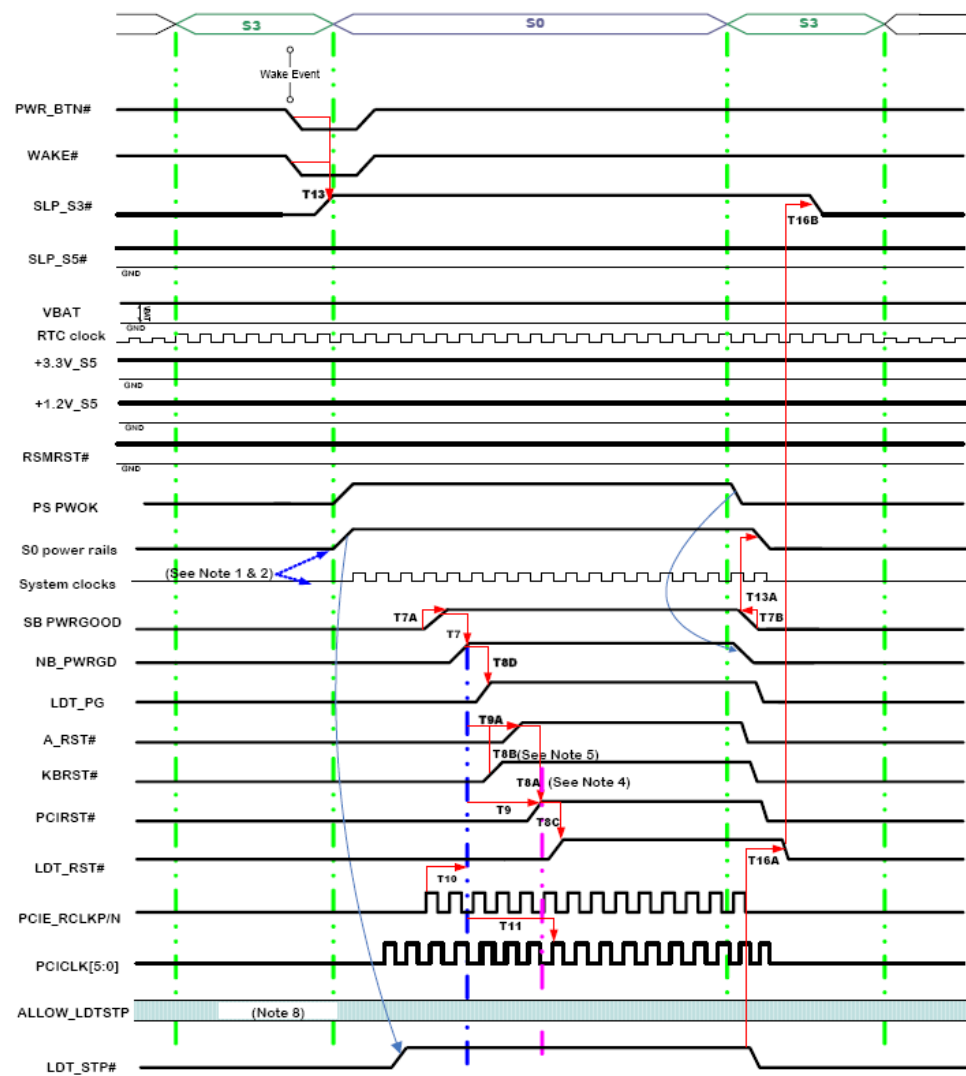


Figure 4-1: SB700 Power Up/Down Sequence

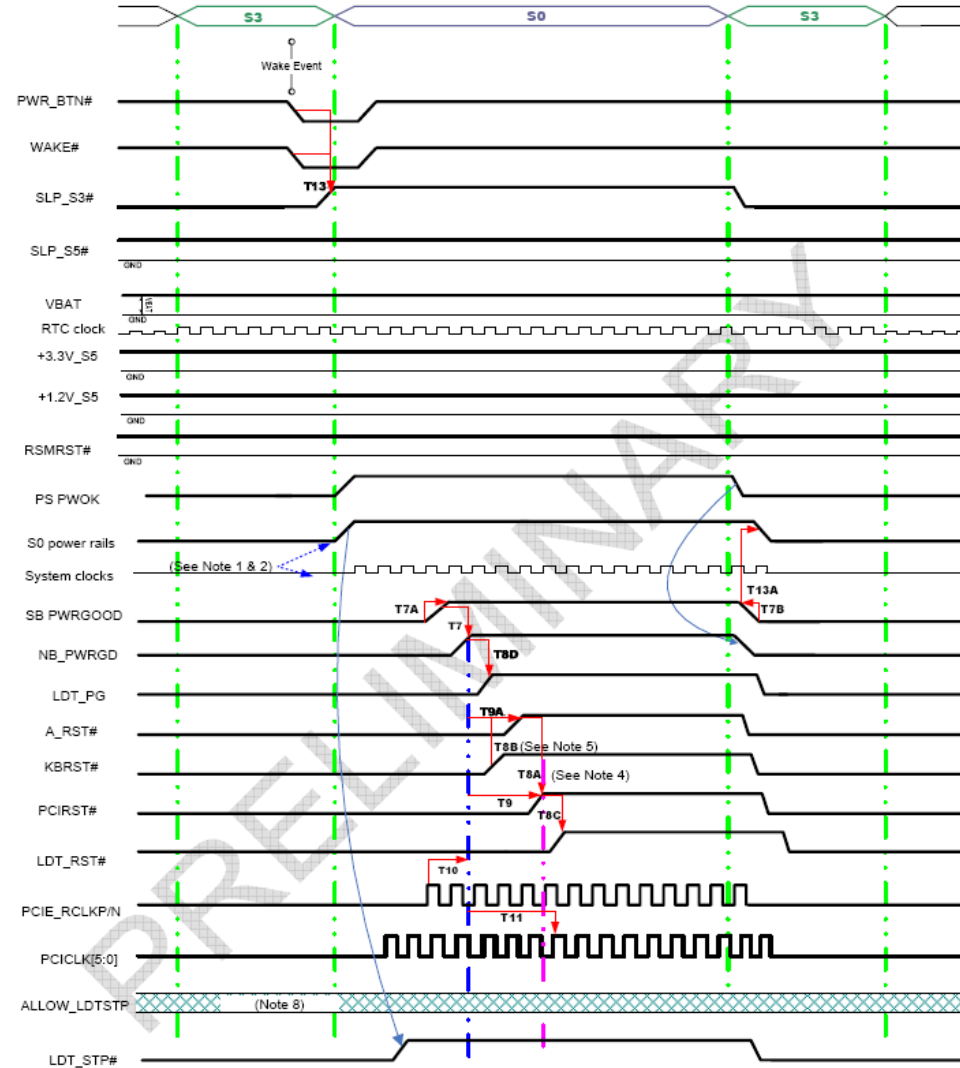


Figure 4-2: SB700 S3/S0 Power Up/Down Sequence

MICRO-STAR IN'L CO., LTD.

Title		Power Sequence	
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ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

CPU PW
12V
+/-5%

2.5V SHUNT
REGULATOR

VRM SW
REGULATOR

1.8V VDD SW
REGULATOR

0.9V VTT_DDR
REGULATOR

VCC 1.2V LINEAR
REGULATOR

VCC 1.1V SW
REGULATOR

1.8V LINEAR
REGULATOR

VCC 1.2V LINEAR
REGULATOR

5V_DUAL &
3VDUAL
REGULATOR ACPI
CONTROLLER

1.2V STB LDO
REGULATOR

3.3V LDO
REGULATOR

LDO
REGULATOR

BAT

PCI Slot (per slot)	
5V	5.0A
3.3V	7.6A
12V	0.5A
3.3Vaux	0.375A
-12V	0.1A

X1 PCIE per	
3.3V	3.0A
12V	0.5A
3.3Vaux	0.1A

X16 PCIE	
3.3V	3.0A
12V	5.5A

USB X4 FR	
VDD	
5VDual	2.0A

USB X6 RL	
VDD	
5VDual	3.0A

2XPS/2	
5VDual	1.0A

GBE	
3.3V 0.5A (S0, S1)	
3.3V 0.1A (S3)	

AM2R2
VDDA 2.5V 0.2A
VDDCORE
0.8-1.55V 110A
DDR11 MEM I/F
VTT 1.75A, VDD 10A
VLD1 1.2V 1.4A

RX/780/RS780
VDDHT/RX 1.1V 1.2A
VDDHT TX 1.2V 0.5A
VDDPCIE 1.1V 2A
NB CORE VDDC
1.1V 7A
VDDA18PCIE 1.8V 0.9A
PLLs 1.8V 0.1A
VDD18/VDD18_MEM
1.8V 0.01A
VDD_MEM 1.8V 0.5A
AVDD 3.3V 0.135A

SB700
X4 PCI-E 0.8A
ATA I/O 0.5A
ATA PLL 0.01A
PCI-E PVDD 80mA
SB CORE 0.6A
CLOCK
1.2V S5 PW 0.22A
3.3V S5 PW 0.01A
USB CORE I/O 0.2A
3.3V I/O 0.45A

AC97 CODEC
3.3V 59.2 mA
3.3V 31 mA

LAN
3VDUAL 7mA
AVDD1.2V 590mA
AVDD2.5V 235mA

SUPER I/O
3VDUAL 20mA
VCC3 1mA
VBAT 1uA

TPM
3.3V 5mA
3VDUAL 25mA

MICRO-STAR INT'L CO., LTD.			
Title Power Delivery			
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MS-7500 0A

06/05/07 Preliminary release

06/15/07

Page 06:R108,R109,R657 AND R658 have been deleted.
Page 15:C542,C597 AND C745 have been added(FOR EMI).
Page 15:R93,R126,R165,R190,R199 R201,R167,R204,R270,R255,R179,R222,R236 and R248 have been deleted(using external CLK-GEN)
Page 15:R175,R179,Q15 and R291 have been added(level-shift for ALLOW_LDTSTOP).
Page 15:R197,R45 and R47 have been deleted(DVI single channel).
Page 18:R338,R339,R340 AND R361 have been deleted(using external CLK-GEN)
Page 19:R176,R211,R214 AND R215 have been deleted(using external CLK-GEN)
Page 19:R242 AND R250 have been deleted.
Page 19:R125 PULLUP 3VDUAL.
Page 19:Add R276.
Page 23:R285,R183,R212,R186,R288,R203R,R189,R366,R357,R352,R351and R344 have been deleted(SB700 HAS 15K INTERNAL PULLUP FOR PCI_AD[30:23])
Page 24:R187,R431,R433 AND R432 have been deleted(using external CLK-GEN)
Page 25:R408,R409,R394,R402,R414,R415,R410,R424,R430,R422 and R423 have been deleted(using external CLK-GEN)
Page 28:R625,R626,R627,R628,R629,R630 have been deleted(using DVI single channel)
Page 31:C771 and C746 have been added(FOR EMI).

06/22/07

Page 06:C157,C158,R99 have been unpopulated,RN3 and R102 have been populated.
Page 06:U51,RN2 have been deleted(for AMD recommend),R74 and J80 have been added.
Page 06:Add R183 and Q17(level-shift).
Page 15:R42,RN43 and Q104 have been deleted,U62 has been added.
Page 15:R172,R175,R181,R192 and R187 have been changed from 3Kohm to 4.7Kohm.
Page 15:R182 has been changed from 2Kohm to 10Kohm.
Page 15:C570 has been changed from 2.2uF to 4.7uF.
Page 17:Add ferrite bead L18,L26,L27,FB19,FB22.
Page 18:L10,L13,L16 and L20 have been populated.
Page 18:C654 and C661have been changed from 10uF to 22uF.
Page 18:C655 and C733 have been changed from 1uF to 2.2uF.
Page 15:R161,R223,R230 and R231 been changed from 10Kohm to 8.2Kohm.
Page 19:R241 has been changed from 5.1Mohm to 20Mohm,R242 has been added.
Page 19: C323,C354,Y4,R168 have been deleted.U4.J21 connected to GND(25M_X1).
Page 20:L29,C412,C924 have been unpopulated.
Page 21:RN36,RN38,Rn35,RN39,Rn40,C372,C511,C535 and C707 have been deleted,R278,R279 and R280 have been added.
Page 21:Add R186 and Q22 (level-shift).
Page 21:SMBDATA1 and SMBCLK1 have been connected U10.
Page 22:Add C394,C513,C748,L22,L36,L41 and EC84,delete C484,C527,C723.
Page 22:C489,C717,C734,C735 and C772 have been changed from 10uF to 22uF.
Page 22:C378,C390,C480,C507,C508,C561,C563,C564,C567,C571,C714,C736,C744 and C747 have been changed from 0.1uF to 1uF.
Page 22:C392,C510,C527,C528 and C721 have been changed from 1uF to 2.2uF.
Page 23:R308,R318 and R333 have been unpopulated,R311 have been populated.
Page 25:Add RN 58,RN59,RN60.
Page 26:RN43,RN47 have been unpopulated.
Page 27:R180,R300 have been changed from 3Kohm to 4.7Kohm,and R89,R91 have been changed from 2.2Kohm to 6.8Kohm.
Page 28:R581~R585,R578~R580 have been changed from 18ohm to 18.2ohm,and R372,R374 have been changed from 2.2Kohm to 6.8Kohm.
Page 28:L21~L24 have been deleted.
Page 31:R177 has been changed from 10ohm to 22ohm.

Page 34:Add R394,C246 and Q45 (AMD recommend).
Page 35:Add R673 (CPU_VDDIOFB_L).
Page 35:Add C723,U22,R430,R30,C707,cb8 and C749 (for PA_SB700AA1).
Page 40:Add U4_X1 (SB HEATSINK).

06/26/07

Page 16:Add R807,R808,C34(for NB MEM_VREF).
Page 18:U6 has been changed from ICS9LPRS472 (MLF 64pin) to ICS9LPRS475 (TSSOP 56pin).
Page 18:R231and R223 have been deleted.
Page 20:L29 has been deleted and CP14 has been added.

06/27/07

Page 34:C245 has been changed from 0.1uF to 4.7uF.(power sequence)

06/28/07

Page 39:Add C290,C297,C298,C315 for EMI.

06/29/07

Page 15:R173,R135,R574,R196 have been deleted and R189,R190,R196 have been added.
Page 16:R148,R162,C202 and C203 have been unpopulated.
Page 19:Add R809,R810,C750,J81 FOR AMD debug.
Page 21:R125 has been deleted.
Page 22:C414 has been populated.
Page 24:R766 and R769 have been populated,R767 and R768 unpopulated. (for HP LAN LED spec)
Page 27:D44,D45 and D46 pin2 connect to VCC3.
Page 36:Add D52,D53.

07/04/07

Page 6:R64 has been unpopulated.

07/05/07

Page 34:Add R399,C247,Q46 for S3 function.

07/09/07

Page 13:Adding C920,C925 0.01,uF stitching capacitors for crossing a split when these signals change different reference layer.
Page 19:Adding C751,C752 0.1,uF stitching capacitors for crossing a split when these signals change different reference layer.
Page 11/07/07
Page 21:Added C387 0.1,uF stitching capacitors for crossing a split when these signals change different reference layer.
Page 32: R575 has been deleted.

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08/01/07

Page 15:Added R93 duo to NC7W207 output pin is op-drain .
Page 23:R325 and R323 have been changed from 10Kohm to 2.2Kohm. (AMD demo schematic update)
Page 29:Add R453 because modify SPI_HOLD# circuit for AMD recommend.
Page 32 :Modify PS_IN# circuit for can't boot issue.
Page 35 :R429 unpopulated and R29 populated for U21 too hot issue.
Page 36 :R430 unpopulated and R30 populated for U22 too hot issue.
Page 38 :Modify PS_ON# and ATX_PWR_GD circuit for can't boot issue.

08/07/07

Page 06:Added AMD Sensor Bus for HP recommend.
Page 15:Added U62.B and R108 for meet powr sequence.

Page 19:Added R248 for 3VDUAL short issue when clean CMOS.
Page 21:C377 and C373 have been unpopulate for meet power sequence.

Page 21:Added PRT_DET# circuit..
Page 25:Added R452,R449 and R451 for modify PE_RST# signal quality.

Page 27:Added NB THERM circuit for HP recommend.
Page 29:Modify Fan-circuit for HP recommend.
Page 32:R335 has been populated for SATA LED.

Page 32:Modify PE_RST# circuit for HP recommend.
Page 34:5V DUAL USB circuit have been populated.
Page 35:R153 has been changed from 220 ohm to 110 ohm for 2.5VREF_NB voltage isn't stable.

Page 37:CPU PWM circuit follow HOUNDS Ver 0B modified.

08/08/07

Page 29:Added FAN-PWM duty cycle inverter circuit for HP recommend.

08/09/07

Page 6:Added C70 for the voltage divider for the gates of the AMD SB-TSI translation circuit needs a decoupling cap.
Page 27: R592 has been populated and R615 has been un-populated for HP recommend .

08/13/07

Page 13: R34 and R36 have changed to 301 ohm 1% resistor when using RS780 for AMD recommend.
Page 14 and 19:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

Page 15: U62 pin5 and R108 pin1 have been connected to 3VDUAL for AMD recommend.
Page 15:Deleted R296. WD_PWRGD signal only connect to R439.

Page 16: C808 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.
Page 17: C598 and C599 has been changed to 0 ohm when RS780 doesn't use side-port memory for AMD recommend.

Page 19:SIO PCICLK has been Changed from PCICLK5 to LPCCCLK1 for AMD recommend.

Page 20: Add R340 .(TEMP_COMM connect to GND for AMD recommend)

Page 21: Deleted R186 and Q22. (SB THRMTRIP# not Implemented)
Page 22: C734,C567,C563,C571,C747 have been un-populated when IDE or flash not using for AMD recommend.

Page 25:PCI-E signal AC coupling have been changed from Y5V to X7R for AMD recommend.

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08/13/07

Page 20:R341 and R319 have been un-populated.(SB700 internal pull-up).
Page 20:Deleted C412 and C924.(SB HW Monitor).
Page 29:Modify Parall port circuit for HP recommend.
Page 29:Added E17(SPI Write Protection) for HP recommend.
Page 29:Modify FAN-PWM duty cycle inverter circuit for HP recommend.
Page 32:Add the detection circuit for 4-pin 12V connector from the power supply for HP recommend.

Page 33:Modify RING Wake Up circuit for HP recommend.

08/14/07

Page 15:R169 has been changed to 3K ohm and populated for RS780.
Page 15:R88 and R178 have been populated for RS780.
Page 15:R198 has been changed to 150 ohm and populated for RS780.
Page 15:R127 has been populated for RS780.

Page 21:Add R186,Q22 ,R199 level shift circuit to U4 THERMTRIP# for HP recommend.

Page 27:D39 has been populated for USB ESB protection.
Page 30:D8,D11,D20,D21,D32,D39 have been populated for USB ESB protection.

Page 31:Add C554 and C569 decouple cap for HP recommend.
Page 32:R335 has been un-populated for HP recommend.
Page 32:R144 has been changed to 470 ohm.
Page 32:U31 has been changed from 75232 to 75185.
Page 33:Net "RDDATA#"pull up resistance value change to 300 ohm.
Page 35:R454 and R455 have been un-populated.R586 has been changed to 4.7K ohm and populated.

Page 35:R21 has been changed to 5.9K ohm for MSI POWER TEAM recommend.
Page 36:R27 has been changed to 5.1K ohm for MSI POWER TEAM recommend.
Page 38:R228,Q23 and R231 have been un-populated.R345 and C645 populated.

08/16/07

Page 39:Added C372,C365,C354 and C364 for EMI.
Page 39:Added CP2,CP3,CP5,CP6,CP7,CP8 and CP9 for EMI.

08/20/07

Page 15:R188 and R254 have been uninstalled for RS780.
Page 21:R217 , R260 and C371 have been deleted.(for I2C signal)
Page 27:Add L6,L21 and L22 for EMI solution.

09/27/07

Page 15:R169 have been uninstalled for RS780.R184 installed 3K

For RS780 2007/09/06
reference AMD demo board
SHINER rev 2.0 C)

Page 35:Changed EC9,EC12,EC14 from 1000uf to 1800uf that MSI POWER TEAM recommend.
Page 36:Changed R25 from 0ohm to 5.1k for MSI POWER TEAM recommend.
Page 37:Changed C807,C301,C819 to 10nf and R702,R718 to 604ohm for MSI POWER TEAM recommend.

10/03/07

Page 35, 36: Change C741, 708 and C732 from 0.01uF to 1uF for DDR power drop issue.
Page 18: Remove R235 for S3 issue.

10/09/07

Page 6: Uninstall R102 and R74 for HP recommended.

10/11/07

Page 12: Change C228, C123 and C231 from 0.1uF to 47pF for EMI.
Page 29: Change C668 from 0.1uF to 47pF for EMI.
Page 9: Install 100pF cap in C609, C194 and C689 for EMI.
Page 9: Change C169 from 180pF to 100pF for EMI.
Page 9: Change C207 from 0.1uF to 100pF for EMI.
Page 9: Install 10pF cap in C188 for EMI.
Page 9: Change C151 from 0.1uF to 10pF for EMI.
Page 9: Change C169 from 180pF to 10pF for EMI.
Page 9: Change C461 from 10uF to 0.1uF for EMI.
Page 9: Change C275 from 0.22uF to 33pF for EMI.

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10/05/07

Page 39: Added C220, C227, C236, C239 and C216 for EMI.
Page 18: Reserved C249 and C241 for EMI.
Page 20: Following AN_SB700AB2.pdf to added 0 ohm series resistor on SATA_TX [5:0]P/N.
R624, R625, R626, R627, R628, R629, R630 and R631
Page 31: Conneted C291, C294, C299, C300, C619, C621, C769 and 770 to GND for Huston EMC lab recommend.

10/08/07

Page 35, 36: Reserved R814, R815, R816, C764, C767 and C768 for Houston lab recommended.
Page 6: Change R107 connected power from VCC_DDR to VBAT.
Page 15: Change the name of a net from SYRESTE# to SYRESET#.

10/12/07

Page 35: Added R588,R632 and Q67 for EN_DDR2 circuit(HP recommend).
Page 35: Added EC47 for USB_PHY POWER.(HP recommend)
Page 15: Deleted R302 ,unpopulated U62 and R108,added R304 and R357 for meet RS780 A12 spec. (AMD recommend)
Page 15: Unpopulated R176,R179,Q15,R170,R171 and Q10;populated R275 and R291 for meet RS780 A12 spec.(AMD recommend)
Page 28: Added L23,L24,L29 and L44 for EMI.

10/16/07

Page 34: Unpopulated EC40 for 3VDUAL issue.(prevent ISL6506CB into OCP state)
Page 35: Populated C742 for meet CPU power sequence. (AMD recommend)
Page 35: Changed R153 from 110 ohm to 220ohm.

10/18/07

Page 6: R107 changed to 10M ohm and R101 changed to 390 ohm for HP recommend.
Page 32: R147 changed pull up to VCC_DDR for HP recommend.
Page 32: Added R633,R634,R637 and R638 (0 ohm) for HP recommedc.

10/19/07

Page 6: Added 0 ohm R199(unpopulated) for HP recommend. (SYS_PWRGD connected to PWROK_PWM)
Page 15 16 : Added two 0.1uF cap (C35,C37) for HP recommend.
Page 34: Added 0 ohm R639(unpopulated) for HP recommend.(PWRGD_SD connected to Q31 pin G)
Page 37: Added 0 ohm R640(unpopulated) for HP recommend.(VCORE_EN connected to U29 pin 24)
Page 34: Added a 4.7uF cap (C791) for HP recommend.
Page 15: Changed R172 and R175 from 4.7K ohm to 39K ohm for AMD RS780 SCL.

Page 18: Changed R218 from 150 ohm to 158 ohm and and changed R229 from 75 ohm to 90.9 ohm for AMD RS780 SCL.

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10/19/07

Page 19: Uninstall R135 for AMD SB700 SCL.

Page 21: Added R268 and R270 for AMD SB700 SCL.

Page 28: Changed R372 and R374 from 6.8K ohm to 15K ohm for AMD RS780 SCL.

Page 32: Install R2 for AMD SB700 SCL.

10/22/07

Page 15: Add R112 and connect U3C.D10 to PCI-E X16 SLOT(B17 B31 B48 B81) for HP recommend.

Page 15: NO_STUFF R81,R84 and R191 and connect A_RST# to SYSRESET# via 0 ohm (R282) for HP recommend.

Page 22: Deleted FB23.

Page 25: STUFF EC28 for HP recommend.

Page 26: Deleted R803,E1 and R438 for HP recommend.

Page 26: CP13,CP26,CP38 changed to 0ohm for HP recomemd (uninstalled).

Page 27: Deleted R615 R593 and R594 for HP recommend.

Page 27: Deleted R599,R602, R597, R598, R595, R596, R609, R608, R605, R606, C680, C679, C678, Q102, Q101 and P12 for HP recommend.

Page 27: Deleted FS9,R159 and R160 for HP recommend.

Page 30: Changed R128,R131,R132 and R136 from 10K ohm to 280 ohm and Changed R123,R130,R133 and R138 from 5K ohm to 330 ohmfor HP recommend.

Page 34: NO STUFF EC40 and STUFF EC57 for HP recommend.

Page 34: Deleted D27 for HP recommend.(5VDUAL).

Page 35: C742 changed from 0.1uF to 1uF.

Page 36: Deleted U22,C723,R430,R30,C707,C749,CB8.

Page 36: Add OV circuit for HP recommend.

10/23/07

Page 15: R304 pin 1 connect to WD_PWRGD for HP recommend.

Page 20: CP14 pin 2 connect to 3VDUAL for HP recommend.

Page 39: J81 chanegd from a header 2*5 to two header 2*3 for AMD recommend .

10/24/07

Page 34: Add two 30K resistors (R803,R817)and one 0.1uF capacitor (C707) to act as a SOFT START circuit for VDDA_25 for HP recommend.

Page 35: R440 change from 1.5Kohm to 1.37K ohm for HP recommend .

Page 36: Add C723 for HP recommend .

Page 21: Add R445 pull up +3VDAUL to USB_OCP#4 for HP recommend .

Page 36: Changed R159 from 10K ohm %5 to 10 ohm 1%and Deleted R182 (same pull up VCC3 to STRP_DATA)

Page 19: Modify battery circuit for HP recommend .

10/25/07

Page 21: Deleted R445 and uninstall R439 for HP recommend.

Page 31: Changed EC42,EC43 from 10uF to 22 uF for HP recommend.

Page 34: Add R641,642 for thermtrip and Vcore issue .

10/26/07

Page 21: R129 changed from 11.8K 1% ohm to 11.3K 1% ohm for SA USB fail.

Page 27: C148,C143,C175 changed from 6pf to 2.2pf and C149,C144,C139 changed from 6pf to 3.3pf and L6,L21,L22 changed from 47nH to 0 ohm for SA VGA signals fail.

Page 35 R440 changed from 1.5K 1% ohm to 7.87K 1% ohm and R426 changed from 1.5k 1% ohm to 8.45K 1% ohm.

Page 36 : R393 , R428 changed from 1.5K 1% ohm to 8.45K 1% ohm and R587 changed from 1.74K 1% ohm to 7.87K 1% ohm and R441 changed from 4.21K 1% ohm to 21K 1% ohm for HP recommend.

Page 38: Add C412,C415,C484 and C494 for SA VCC5 fail.

10/29/07

Page 19: Add R140 for HP recommend.

Page 21: Add R271 and R258 for HP recommend.

Page 34: Add Q92 for HP recommend.

Page 36: Update NB OV circuit (add R167 R160 R113 and Q96) for HP recommend.

10/30/07

Page 21: R129 changed from 11.3K 1% ohm to 11.8K 1% ohm for AMD recommend.

Page 36: Update NB OV circuit (R160,R113,R167,R159,R431,R68 change value) for HP recommend.

11/06/07

Page 19: Add SW50 switch operation table.

11/08/07

Page 15: Q4 changed from 2N7002 to P8503 for HP request.

Page 36: for HP request
1.Stuff R113 with 0 ohm
2. Un-stuff Q96
3. Un-stuff R159
4. Change R167 to 10K 1%

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11/28/07

Page 34: Add Q98,Q101,Q102,R383,R402 for get 4 beeps when a crowbar is detected for HP recommend.

11/29/07

Page 35: Update VTT power circuit for meet AMD spec.

12/04/07

Page 06: uninstall Q17,R28,R183 and install R199 for HP recommend.

Page 34: Add R643,R644 for HP recommend.

Page 34: Uninstall Q33,R436,D17 and install R639 for HP recommend.

Page 36: R167 change from 10K ohm to 2K ohm for HP reconnamd.

Page 37: uninstall R794,Q72,R690,R691,R654 and install R640 for HP recommend.

12/06/07

Page 15: Del R190, R196 (DFT_GPIO4/5)pull up R for HP recommend.

Page 15: Add C678 for AVDD by pass cap ; Add C679 for AVDDI by pass cap that HP recommend.

Page 27:Remove C122 and C135 for HP recommend.

12/10/07

Page 27: C792,C793 changed from 0.1UF to 0 ohm and R91,R89 change from 6.8K ohm to 2.2K ohm and R686,R687 change from 33 ohm to 22 ohm

Page 35: Change R593, R594 value from 20K to 1K; C749 from 1uf to 0.1uf.

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12/11/07

Page 27: NO STUFF C792 and C793 for HP recommend.

12/12/07

Page 27: STUFF C792 and C793 for HP recommend.

12/14/07

Page 27: L2-4,L6,L21,L22 C139,C144,C149,C175,C143,C148.,R91,R89 change value for SA report

12/19/07

Page 37: R725 changed to 2.8K 1%,R720 changed to 2.49K 1% , C801 changed to 150pf for meet CX state power spec .

12/20/07

Page 37: R725 changed to 2.2K 1%,R720 changed to 2K 1% , C801 changed to 47pf for meet CX state power spec .

Page 37: STUFF EC64,EC65 and EC67 for CX state power spec.

Page 8: STUFF C448,C453,C458,C466,C687,C688 for CX state power spec.

Page 15:Unstuff R41,R44,R46,R47 for reference AMD borard SHINER rev 2.3 c and TILAPIA rev 0.2.

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12/24/07

Page 6: Add R125,R126 for AMD recommend.

01/04/08

Page 35:R429 change from 0 ohm to 100 ohm for simulate the 10mA minimum loading, avoid S5 state USB_PHY power rail light loading.

01/18/08

Page 28:R578~R585 change from 18.2 ohm to 0 ohm for HP recommend.

01/25/08

Page 20:R624~R631 change from 4.99 ohm to 0 ohm for HP recommend.

Page 28:R578~R585 change from 0 ohm to 18.2 ohm for HP recommend.

02/15/08

Page 18:C650 change from 22pf to 27pf for HP recommend.

Page 29:R405 change from 10K ohm to 1K ohm for HP recommend.

Page 40:Add DVI gasket J70_1.

02/19/08

Page 04: Update SB700 GPIO table.

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10/03/08					
Page 31: C644 change to 1uF/25V/X7R/0805 and connect to AGND.					C
Page 39: C667 empty and C659 install 0 ohm/0603.					
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Page 31: C644 change to 1uF/25V/X7R/0805 and connect to AGND.

Page 39: C667 empty and C659 install 0 ohm/0603.

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10/03/08

Page 31: C644 change to 1uF/25V/X7R/0805 and connect to AGND.

Page 39: C667 empty and C659 install 0 ohm/0603.

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